

VME Intensity Monitor - Support #12824

Milestone # 12944 (New): New DCCT V2.1 Firmware Driver

MIDCCT Initialize Registers

06/01/2016 10:16 AM - Roger Tokarek

Status:	Closed	Start date:	06/01/2016
Priority:	Normal	Due date:	
Assignee:	Roger Tokarek	% Done:	20%
Category:	DCCT	Estimated time:	24.00 hours
Target version:		Spent time:	0.00 hour
Description			
Register default values need to be set on startup. See Wiki MIRR DCCTs .			

History

#1 - 06/01/2016 10:39 AM - Roger Tokarek

- Estimated time changed from 16.00 h to 24.00 h

Steps:

1. Translate handwritten Engineering request into Excel spreadsheet.
2. Create a Wiki entry.
3. Find and gather references, notes and Excel into Wiki. Create Defaults Table.
4. Identify missing components: eg register sizes, missing default values, coefficients.
5. Identify and understand software implementation requirements.
6. Create and implement code.

#2 - 06/01/2016 05:21 PM - Roger Tokarek

- % Done changed from 0 to 20

Status:

- Excel spreadsheet created.
- Wiki created: [MIRR DCCTs/MI DCCT Support](#).
- Transfer Excel spreadsheet values to [MI DCCT Support](#), "Main Injector DCCT Default Startup Values".

#3 - 06/01/2016 05:28 PM - Roger Tokarek

Notes:

1. There are 64 FIR coefficients to be transferred for each FIR Filter.
2. Nios requires a wait period during FIR coefficients transfer. Check HW_Busy register 0x008c (D8) before reading data.
3. The vme_a32_qsys_pointer is at 0x0088 (D32).

#4 - 06/02/2016 12:01 PM - Roger Tokarek

Because we are temporarily supporting two different DCCTs (ANUB - old firmware, MIDCCT new firmware) with the same class DcctDrv, and because there are register conflicts between them, we can use the "m-command" to set the MIDCCT registers for now. This is a hack and is temporary.

The following is added to midcctstartup in git branch midcct_12824.

```
# set the MIDCCT default startup values (hack for now!)
# set in order as presented by engineering:
# see Redmine Support #12824

m 0xfbff2000+0xDC, 4
0X00001FD8
.
m 0xfbff2000+0xE2, 2
0X105B
.
m 0xfbff2000+0xE0, 2
0X0000
```

```

.
m 0xfbfff2000+0xE6,2
0X147B
.
m 0xfbfff2000+0xE4,2
0X0000
.
m 0xfbfff2000+0xEA,2
0X0000
.
m 0xfbfff2000+0xF2,2
0X2028
.
m 0xfbfff2000+0xED,1
0X01
.
m 0xfbfff2000+0xEC,1
0X05
.
m 0xfbfff2000+0xFE,1
0X04
.
m 0xfbfff2000+0xF6,2
0X0000
.
m 0xfbfff2000+0xF0,2
0X5333
.
m 0xfbfff2000+0xFA,2
0X0000
.
m 0xfbfff2000+0xF4,2
0X0001
.
m 0xfbfff2000+0xF8,2
0X7FFF
.
m 0xfbfff2000+0xFF,1
0X00
.
m 0xfbfff2000+0xFC,2
0X0728
.
m 0xfbfff2000+0x103,1
0X00
.
m 0xfbfff2000+0x102,1
0X0A
.

```

#5 - 06/06/2016 10:36 AM - Roger Tokarek

Fir Filter Coefficients

Three FIR that need to be initialized, two of the three are identical.
 DC and DAC0 FIR Coefficients = first 64 taps set to 32767 (x7FFF); all others = 0
 AC FIR Coefficients = first tap set to 32767 (x7FFF); all others = 0

#6 - 06/16/2016 04:23 PM - Roger Tokarek

- Parent task set to #12944

#7 - 06/17/2016 09:52 AM - Roger Tokarek

Additional MIDCCT initialization

DAC2 CIC decimation rate = 1176.
 DAC0 CIC decimation rate = 8232
 DAC0 CIC gain = 0
 DAC0 FIR gain = 3
 DAC0 FIR has 64 coefficients whose values are all 9.

Not yet implemented June 17, 2016

#8 - 08/03/2016 01:17 PM - Roger Tokarek

- Status changed from New to Closed