Overview of the Front End Electronics for the MINOS Near Detector

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1. Introduction

The electronics for the Near Detector will be different from that used in the Far Detector. In principle, the electronics could be the same, but several considerations have made it more advantageous for the two systems to be different. The primary consideration is that the instantaneous event rate will be much greater in the Near Detector than in the Far Detector. The Main Injector is being designed for high beam intensities that can produce one or more event in the Near Detector in each RF bucket during the spill. In order to reconstruct each event accurately, it is necessary to be able to associate every event with a particular RF bucket. This requires very fast electronics, capable of digitizing at the 53 MHz RF frequency. Furthermore, since the spill will last for only 10 microseconds, it is desirable that there be no dead-time during the spill, so that every event that occurs during the spill is measured and recorded. The electronics for the Far Detector does not need to operate at this rate, and it would be overkill to put fast electronics there. For a given dynamic range and accuracy, fast electronics with low dead-time is generally more expensive than slow electronics. Since there are three times more channels in the Far Detector than in the Near Detector, there is a significant savings in having fast electronics only in the Near Detector. Of course, the systematic differences between the two detectors must be understood, but previous experience with upgrading the CDF detector electronics without changing the detector has shown that systematics associated with different electronics can be understood to the 1% level with careful calibration and study. This should be adequate for the MINOS experiment.

The DAQ system will be able to operate in three different modes:

(1) *Single Turn Extraction Mode.* The trigger is a spill signal from the main injector. Data will be collected for every RF bucket during the 10 microsecond spill and will be stored in FIFOs on front-end cards. Collection of data from the front-end FIFOs will be deferred until after the spill. The Data Acquisition (DAQ) system will receive zero-suppressed data. Events will be time-stamped according to the RF bucket with which they are associated This mode is dead-timeless, with respect to the spill time.

(2) *Cosmic Ray Mode.* Cosmic ray data will be collected during the one-second intervals between spills. Data from a few RF buckets will be stored on receipt of a local, prompt trigger (e.g., a discriminated dynode signal). Front-end FIFOs will be read out as soon as data is available. The DAQ system will receive zero-suppressed data. Dead-time will be small.

(3) *Resonant Extraction Mode.* As in Cosmic Ray Mode, data from a few RF buckets will be stored on receipt of a trigger from a dynode discriminator, but FIFO readout will be deferred until the end of the spill. The DAQ system will receive zero-suppressed data. This mode will be dead-timeless as long as FIFOs do not overflow. (In principle, FIFO readout might be permitted to occur during the spill, but it remains to be seen whether noise from this asynchronous digital traffic will be acceptable.)

The requirements on the electronics for the Near Detector are quite stringent. The electronics must be capable of accurately measuring the charge from a photodetector that occurs from 1-2 photoelectrons. To accomplish this, the electronics should have enough resolution to resolve the charge from a single photoelectron above the noise floor of the electronics. An event from the beam might produce a shower, which can produce ~150 photoelectrons. In addition, there can be as much as a 3-to-1 gain variation in the pixels from the photodetectors. With all these factors, the electronics must have a dynamic range of 12 bits. As described above, the electronics must have low dead-time, and be capable of digitizing at 53 MHz. To achieve this performance, the ASIC Design Group at Fermilab has developed a custom integrated circuit that has been used in several applications to date. The device, called QIE, has been used by KTeV, CDF, and is being planned for CMS. It can operate at 53 MHz, is pipelined so that there is no intrinsic dead-time, and has a dynamic range of 16 bits. It is planned to modify this device to optimize it for the MINOS Near Detector front end electronics.

The following sections describe the system in detail. A list of general system requirements is presented in Section 2. A detailed description of the QIE is presented in Section 3, followed by a description of the functional blocks in Section 4. In Section 5, a description the modes of operation is given, including calibrations. A discussion of the physical implementation is presented in Section 6.

2. System Requirements

The following is a list of the general requirements on the electronics for the Near Detector:

1. Least Count Resolution

   It is expected that the photodetectors will operate at a maximum gain of 1E6. The gain of the worst-case pixel may be a factor or 3 lower. The electronics must accurately measure the charge from a single photoelectron, with enough resolution to be above pedestal noise. A single photoelectron produces ~50 fC for the lowest-gain pixels. The least count resolution of the QIE is 7.5 fC. A single photoelectron would then register ~7 ADC counts above pedestal for the low-gain pixels. (We are exploring the possibility of modifying the QIE to have a least count resolution of 3 fC, in which case a single photoelectron would register ~15 ADC counts above pedestal. This is an area of R&D.)

2. Largest Signal and Dynamic Range

   The largest signal is expected to be ~25 mips. Each mip produces ~6 photoelectrons, which is equivalent to ~24 pC of charge for the highest gain pixels at 1E6. This gives a minimum dynamic range of 3200, or 12 bits.

3. Digitization Rate

   The system must be capable of digitizing at 53 MHz, the RF frequency of the Main Injector. In particular, the system must be capable of recording events that occur in successive RF clocks during the spill.

4. Dead-time

   There must be no dead-time from the electronics during a spill. The electronics must be capable of measuring and recording all events which occur during the ~10 uS spill duration.

   For measuring cosmic rays, a live time of 80% is desirable. Cosmic ray data will be acquired during the one-second interval between spills.

5. Time-stamping

   All events will be time-stamped to a resolution of the RF clock (~19 nS).

6. Zero-Suppression

   All events will be zero-suppressed. Only channel data above a programmable threshold will be read out. (An option under discussion is to read out data from several clock cycles around an event above threshold.)

7. DC Current Monitoring

   Capability will be provided for reading out DC current from radioactive sources.

3. Description of QIE

The analog signal processing circuitry used in the front end electronics is based on a custom integrated circuit developed at Fermilab. This device is called the QIE (Charge (Q) to Current (I) Encoder.) It was originally designed for the SDC, and later adapted for the KTeV experiment at Fermilab [1-2]. Two versions have also been designed for CDF [3]. It is fabricated in a 2 um, double-metal, double-poly process, and employs both CMOS and bipolar transistors.

The device is capable of continuous analog processing at 53 MHz with no dead-time. This is accomplished by pipelining the analog operations. The device has a wide dynamic range, and uses a "floating point" format to accomplish this. There are 8 binary-weighted ranges in the device, and circuitry inside the QIE automatically chooses the "range of interest" for digitization. The 8 ranges are represented by 3 Range Bits, which are provided as an output from the QIE. The QIE puts out an analog voltage associated with the range of interest. An external ADC, operating at the same clock speed, performs the digitization. The combination of the two devices produces a continuous stream of digitized data without dead-time. If the ADC has 8 bits, then the total dynamic range of the combined devices is 16 bits (8 ADC bits, with 8 ranges.) The device has excellent noise and linearity characteristics, and is well matched for use with an 8-bit ADC. A block diagram of the QIE is shown in Fig. 1.

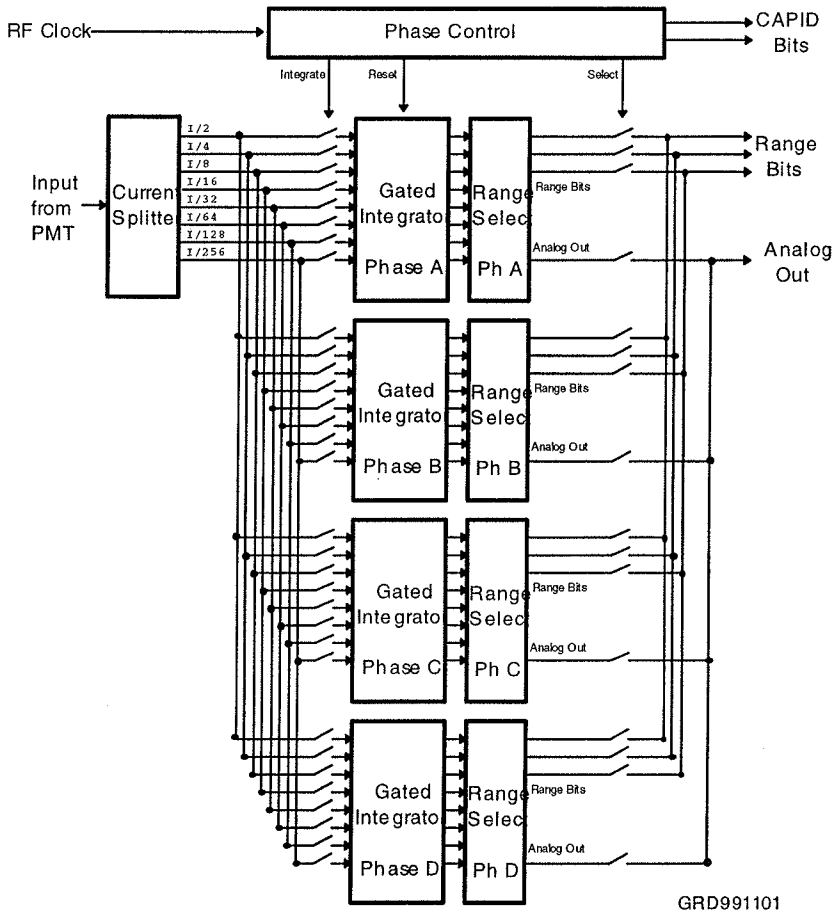


Fig. 1. Block Diagram of the QIE

The heart of the QIE is circuitry called a "current splitter." This is a gated integrator, which splits the input current from the detector into 8 binary-weighted ranges. This is accomplished by using 128 identical NPN transistors, as shown in Fig. 2. The emitters of all transistors are connected together at the input node, which is also connected to a bias current source. With no input current coming in from the detector, the bias current divides itself evenly between the 128 transistors. The collectors are grouped together in binary fashion. The group designated as "I/2" in Fig. 2 has the collectors of 64 of the 128 transistors connected together. Thus, the current into these collectors is equivalent to 64/128 of the bias current, or I/2. This is called the I/2 Range. Similarly, the I/4 Range sources 1/4 of the bias current, the I/8 Range sources 1/8 of the bias current, etc. The last two ranges use a single transistor each. Both the I/128 Range and the I/256 Range source 1/128 of the bias current. The I/256 Range is handled specially, and will be described shortly. Note that the sum of the current fractions from all the ranges equals 1.

To begin the signal acquisition sequence, assume that the integrating capacitors in Fig. 2 have already been reset, so that they contain no initial charge. When the Sample & Hold (S&H) switch connecting the collectors to the integrating capacitor on the I/2 Range is closed (or gated) for period T, the voltage developed on the I/2 integrating capacitor is:

$$V_{I/2} = [\,(I_{BIAS} / 2) * T\,] / C$$

Similarly, the voltage produced on the integrating capacitors for the other ranges is:

$$V_{I/4} = [\,(I_{BIAS} / 4) * T\,] / C = V_{I/2} / 2$$
$$V_{I/8} = [\,(I_{BIAS} / 8) * T\,] / C = V_{I/2} / 4$$
$$V_{I/16} = [\,(I_{BIAS} / 16) * T\,] / C = V_{I/2} / 8$$
$$V_{I/32} = [\,(I_{BIAS} / 32) * T\,] / C = V_{I/2} / 16$$
$$V_{I/64} = [\,(I_{BIAS} / 64) * T\,] / C = V_{I/2} / 32$$
$$V_{I/128} = [\,(I_{BIAS} / 128) * T\,] / C = V_{I/2} / 64$$

For the I/256 Range, the integrating capacitor is doubled, to give a voltage of:

$$V_{I/256} = [\,(I_{BIAS} / 128) * T\,] / 2C = V_{I/2} / 128$$

This shows how the bias current that is split into binary-weighted fractions produces binary-weighted voltages on the sample and hold capacitors. If additional current is pulled from the input node, for example by a photodetector in response to an event, the signal current is split in the same way, adding additional voltage onto each integrating capacitor.

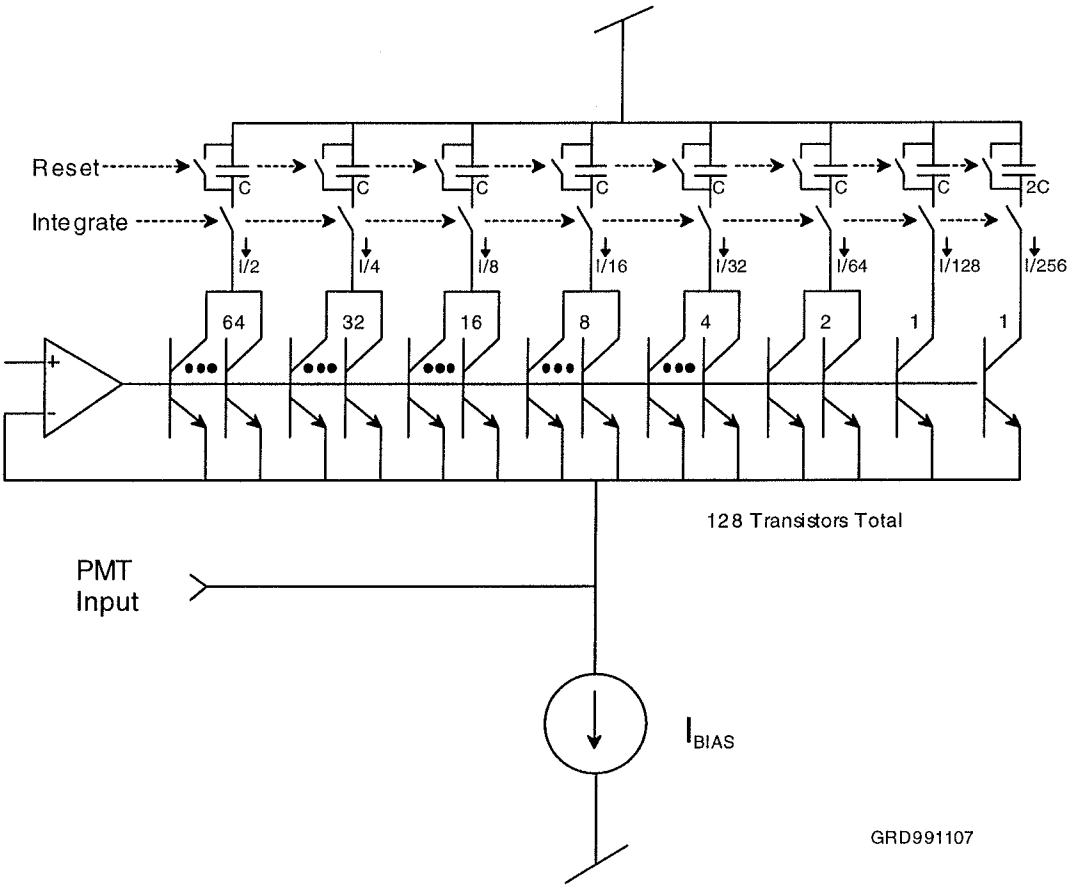


Fig. 2. Block Diagram of the Current Splitter

The QIE has four phases of operation, as shown in Fig. 3. The phase just described is the Integration Phase. At the end of this phase, all of the S&H switches are opened, and the resulting voltages are held on the integrating capacitors for further processing. A buffer drives out the voltage from each capacitor to a set of comparators, which selects one of the voltages for digitization. This is the Range Select Phase. The biasing is arranged such that one and only one of the ranges will be within the digitization range of the ADC. From this, a binary representation of the selected range is produced for output. This phase takes one clock period.

Once a range has been selected for digitization, the Range Bits are presented on output pins, and the voltage on the corresponding integration capacitor is switched to the analog output of the device, making it available to the ADC for digitization. Allowing for settling, the ADC can be clocked at the end of this clock cycle. This is the Digitization Phase, and takes one clock period.

After the ADC has digitized, the Range Bits are appended to the ADC bits to form the floating-point data word. Next, all of the integrating capacitors are reset to prepare them for the next integration cycle. This is accomplished by briefly closing a switch around the integrating capacitor. This is the Reset Phase, and takes one clock cycle.

Note that after the Integration Phase, it takes 3 additional clock cycles to process the signal acquired on the integration capacitors and prepare for the next integration cycle. Without additional circuitry, the device would be dead 75% of the time. To accomplish dead-timeless operation, there are actually 4 sets of circuitry on each range, as shown in Fig. 1. Each capacitor on a range is part of an overall phase of operation for the device, i.e. while one set of capacitors (one from each range) is integrating, another set is being selected for range, another set is being digitized, and the other set is being reset. The phase of operation changes with each clock cycle in round-robin fashion. In order to keep track of second order effects, a two-bit identifier is appended to each data word, called the CAPID Bits. These bits identify the set of capacitors that were used to acquire and process a particular data word. This circuitry effectively pipelines the device, and produces dead-timeless operation. Thus, a QIE data word consists of 13 bits:

CAPID[1:0]
RANGE[2:0]
ADC[7:0]

Because the QIE usesa binary -weighted scheme to acquire and process charge signals, the transfer function for the device (plot of ADC bits produced versus input charge) has a unique shape. This is shown in Fig. 4. Each line segment represents the response of an integrating capacitor for a particular range. Note that this figure shows the response of one phase (i.e. always reading out the same CAPID.) There are 4 such plots for each QIE channel.

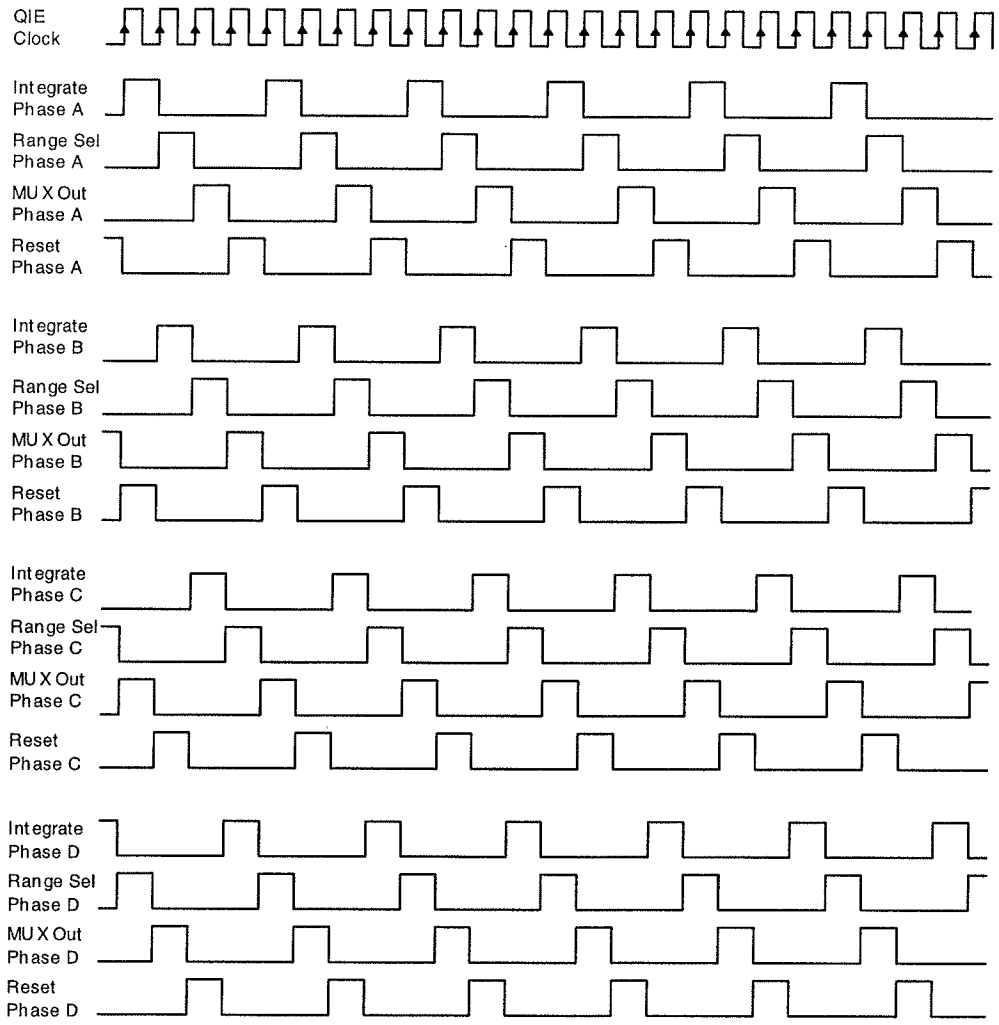


Fig. 3. Timing Diagram for the QIE

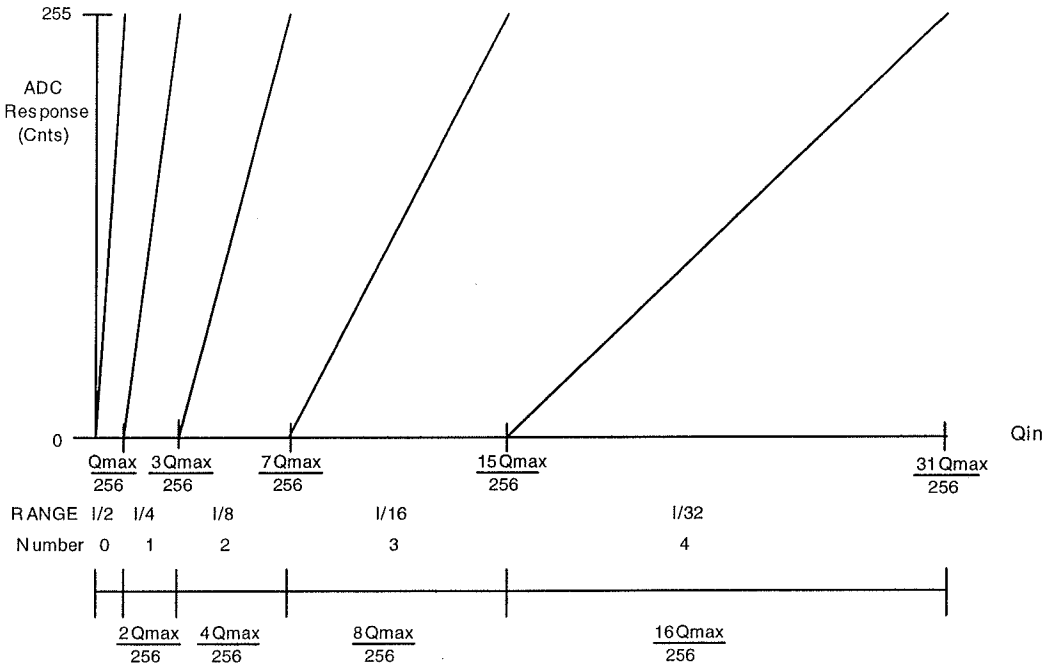


Fig. 4. Ideal QIE Transfer Function
(Ranges 5-7 not shown.)

The principle behind the QIE is that the device always produces a digitized value which has ~0.4% (8 bit) accuracy over the entire range of operation. Before input charge can be reconstructed, the QIE response must be measured. This is done by first calibrating the QIE before a data acquisition run, thereby obtaining a slope and offset for each range and for all phases. Note that there are 32 integrating capacitors in the device, so the calibration procedure produces 64 calibration constants for each device. This calibration accounts for mismatches in the chip. Each capacitor can be a little different, which can give gain errors. In addition, each capacitor has a buffer and a comparator associated with it, which can give offset errors. The capacitors tend to be matched to ~1%, and comparator and buffer offsets match to ~10 mV. If a high degree of accuracy is required to reconstruct the input charge from the floating point QIE word, then all capacitors need to be measured and calibrated separately. The calibration procedure will be described in a later section.

4. System Architecture

4.1 Overview of System

There are two primary parts to the system. The Front End Crates contain the QIE electronics. They are situated very close to the photodetectors, which is desirable in order to reduce noise degradation associated with long signal cables. Digitized data is held in FIFOs in the Front End Crates pending a readout cycle. When a readout cycle is initiated, the digitized data is sent to VME Readout Crates, which acts as a data funnel, collecting fragments of events together for further processing. The data is zero-suppressed and reformatted, and put into holding buffers, where it can be accessed by a VME computer which resides in each crate. The computer collects data from all VME readout boards in the crate, time orders the data, and then sends it to the DAQ system for event building and selection.

Subdividing the primary parts, the front end electronics has 6 components. These are introduced below, and described in detail in the sections that follow. A block diagram showing how the components fit together is shown in Fig. 5.

The heart of the system is the QIE custom ASIC, which was described in Section 3. The QIE itself is dead-timeless, and digitizes at the RF clock frequency of 53 MHz.

The QIE is mounted on a daughter board called the MENU Module. It has a format similar to a memory SIMM. These boards also contain the ADC, data buffering, and circuitry for performing electronics calibrations and source monitoring. Data is digitized and stored on these modules, and made available for readout when addressed.

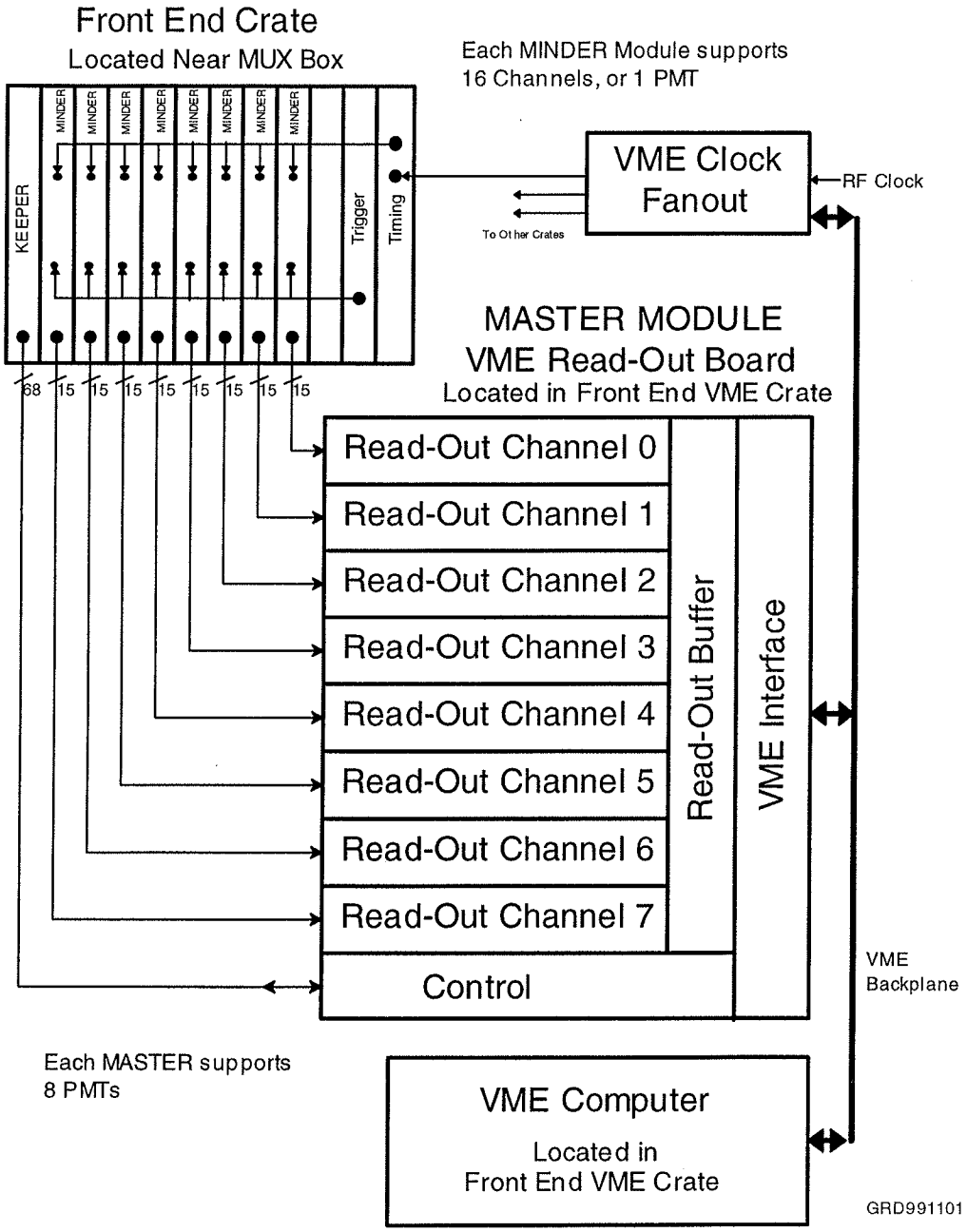


Fig. 5. Block Diagram of the Front End Electronics

MENU Modules are mounted on a motherboard called the MINDER Module. These boards contain support circuitry for the MENU Modules, including time-stamping, and they control the multiplexing of data from each MENU Module during read-out. This board has a 6U format, and resides in a 6U Euro-style crate. These crates, called the Front End Crates, are mounted close to the photodetectors.

When data is ready for readout, it is transmitted from the MINDER Modules to a readout board called the MASTER Module, which resides in a 9U VME crate. Since the data being transferred is digital, the VME crates can be far away from the Front End Crates. The MASTER Module receives data from up to 8 MINDER Modules. The MASTER Module also provides control for the MINDER Crate. There is a simple controller in the MINDER Crate called the KEEPER, which is controlled by the MASTER. One of the functions is to control a DAC that resides on the KEEPER. The DAC is used for calibrating the QIEs. The MASTER also sets up calibration runs, pedestal runs, and other diagnostic functions through communication with the KEEPER.

A clock distribution system distributes clock signals to the Front End Crate. The Master Clock Module receives the RF clock, and fans it out to the Front End Crates. It also transmits two other signals. One signal resets the time-stamping circuits on the MINDER Modules. The other is a signal indicating that a spill is in progress. Both of these must have precise timing with respect to the RF clock. These signals are fanned out to a Clock Fan-Out Board, which resides in the MINDER Crate. This board receives the timing signals, and fans them out, point-to-point, to all of the MINDER Modules in the crate.

A module containing dynode signal discriminators also resides in the Front End Crate. When a dynode signal is received, this TRIGGER Module sends a signal directly to the appropriate MINDER. This would be the cosmic ray trigger. It could also be used for triggering when resonant extraction is achieved, but it may be desirable to construct a more complex trigger for this type of operation.

4.2 QIE Daughter Board

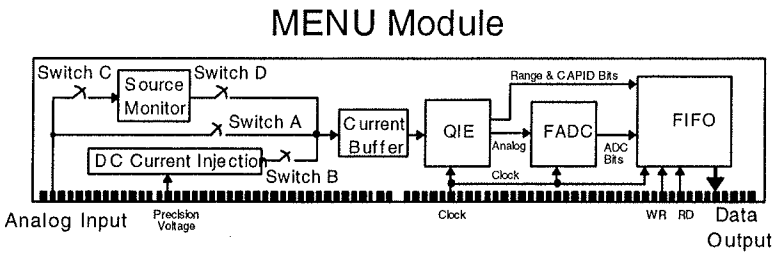
Each QIE is mounted on a small board called the MENU Module (MINOS Electronics for Neutrinos.) These are configured as daughter boards, which reside on the MINDER Modules in the front end crate. A block diagram of a MENU Module is shown in Fig. 6. The board contains the QIE, an 8-bit ADC, and a FIFO for storing the data. The board also contains circuitry for measuring source current, circuitry for injecting DC current into the QIE for performing electronics calibrations, and a current buffer.

A current buffer provides impedance matching between the QIE and the photodetector. The primary function is to terminate the transmission line between them, reducing the reflections that might otherwise occur. This is especially important given the fast edges of a single photo-electron signal. The input impedance of the QIE is dynamic, a function of the instantaneous input current. The buffer is required when the signal cables become long, as was the case in the implementation for CDF. For MINOS, the signal cables will be 1 meter or less, but given the short integration period of the RF clock, and also the requirement of measuring single photoelectrons, the current buffer is thought to be necessary.

A simplified schematic of the current buffer is shown in Fig. 7. It is essentially a common base configuration. The intrinsic input impedance is a fraction of an ohm. The series input resistor controls the termination impedance. The input current is pulled through the emitter, into the collector from the QIE. The intrinsic noise of the circuit, referenced to the input, has been measured to be ~2 nV/SQRT(Hz). The noise from the current buffer represents a fraction of an equivalent LSB of the QIE, for a coaxial signal cable of 1 meter in length.

The QIE will be calibrated using a voltage-controlled DC current injector. The circuit, called a Howland Current Source, is shown in Fig. 8. It has been used successfully in CDF, to high precision. This circuitry will provide the means for obtaining slopes and offsets for all of the ranges and phases of the QIE, which are needed to linearize the QIE data. The DC current injector can also be used for diagnostic purposes.

A simplified circuit diagram for the radioactive source monitor is shown in Fig. 9. This circuit contains an integrator with a large time constant, and a Howland voltage-to-current converter on the back end. This circuit has also been implemented successfully for CDF. It is low-noise, accurate, and low-cost. In the event that source monitoring is not needed in the Near Detector, it is easy to leave this circuit out of the assembly of the board.



MODE	Switch A	Switch B	Switch C	Switch D
Normal DAQ	Closed	Open	Open	Open
DC Current Inj	Open	Closed	Open	Open
Source Monitor	Open	Open	Closed	Closed

GRD991101
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Fig. 6. Block Diagram of MENU Module

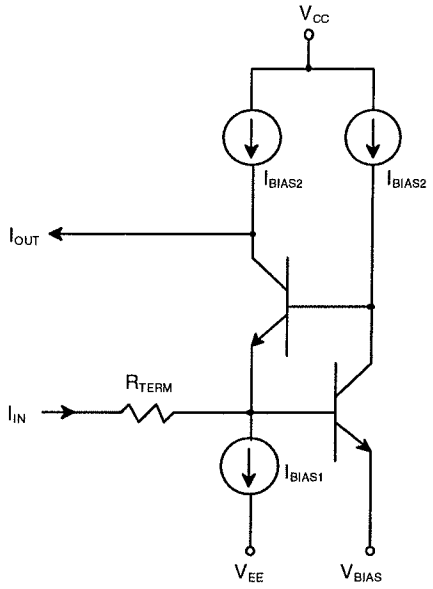

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Fig. 7. Simplified Schematic of the Current Buffer

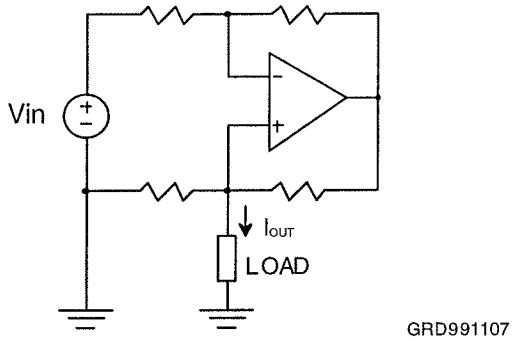

Fig. 8. The Howland Voltage-Controlled Current Source

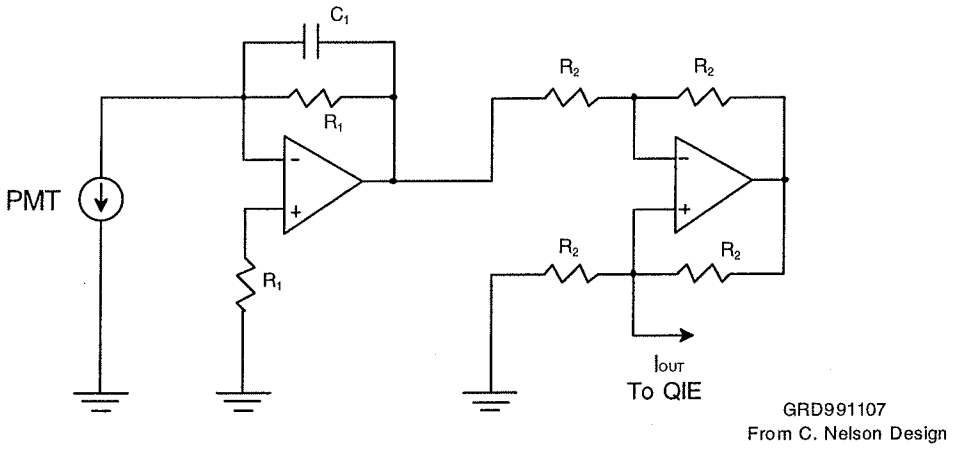

Fig. 9. The Radioactive Source Monitor Circuit

The switches in Fig. 6 are controlled through system commands from the VME readout board. The table in Fig. 6 shows how the switches are configured in normal data mode, calibration mode, and source monitor mode.

As described above, the QIE generates Range Bits and CAPID Bits, along with an analog voltage, on every clock cycle. The ADC digitizes the analog voltage to 8 bits. The resulting 13 bits of data (8 ADC bits, 3 range bits, 2 cap ID bits) form the data word for a given clock cycle.

The QIE and ADC are clocked continuously at 53 MHz. Data is transferred to the FIFO when a control signal from the MINDER is asserted. The conditions under which data is written into the FIFO will be described later. The FIFO is 1K words deep. If the FIFO ever fills up, the FIFO_FULL flag is asserted, and no more data can be written until the condition is cleared. This error condition will be reported to the system.

Data is read from the FIFO under control from the MINDER board, which is described in the next section. Due to limited space on the MENU Module, the FIFO cannot have simultaneous read/write capability, so the writingof data into the FIFO must be stopped during data readout. The implications for dead-time will be addressed in Section 5.

4.3 Front End Mother Board

The motherboard that hosts the MENU Modules is called the MINDER Module (MINOS Near Detector Electronics Readout.) It contains 16 MENU Modules, and services one 16-channel photodetector. A block diagram is shown in Fig. 10.

The MINDER Module has 3 primary functions: (1) it handles the time-stamping of data; (2) it controls the multiplexing of data from the MENU Modules to the VME readout board; (3) it provides power, control, and interface functions for the operational support of the QIEs.

The time-stamping is implemented on the MINDER Module using a 26-bit Grey-code counter, which counts RF clocks. This provides over 1 second of time-stamping at the RF clock frequency. The counter is reset by a signal from the Clock System (See Section 4.7), and the counter value is incremented by the RF Clock signal. When a trigger occurs, the value of the counter is put into a register, and becomes part of the header word that is sent to the VME readout board at the start of data transfer. There is one time-stamp per data record.

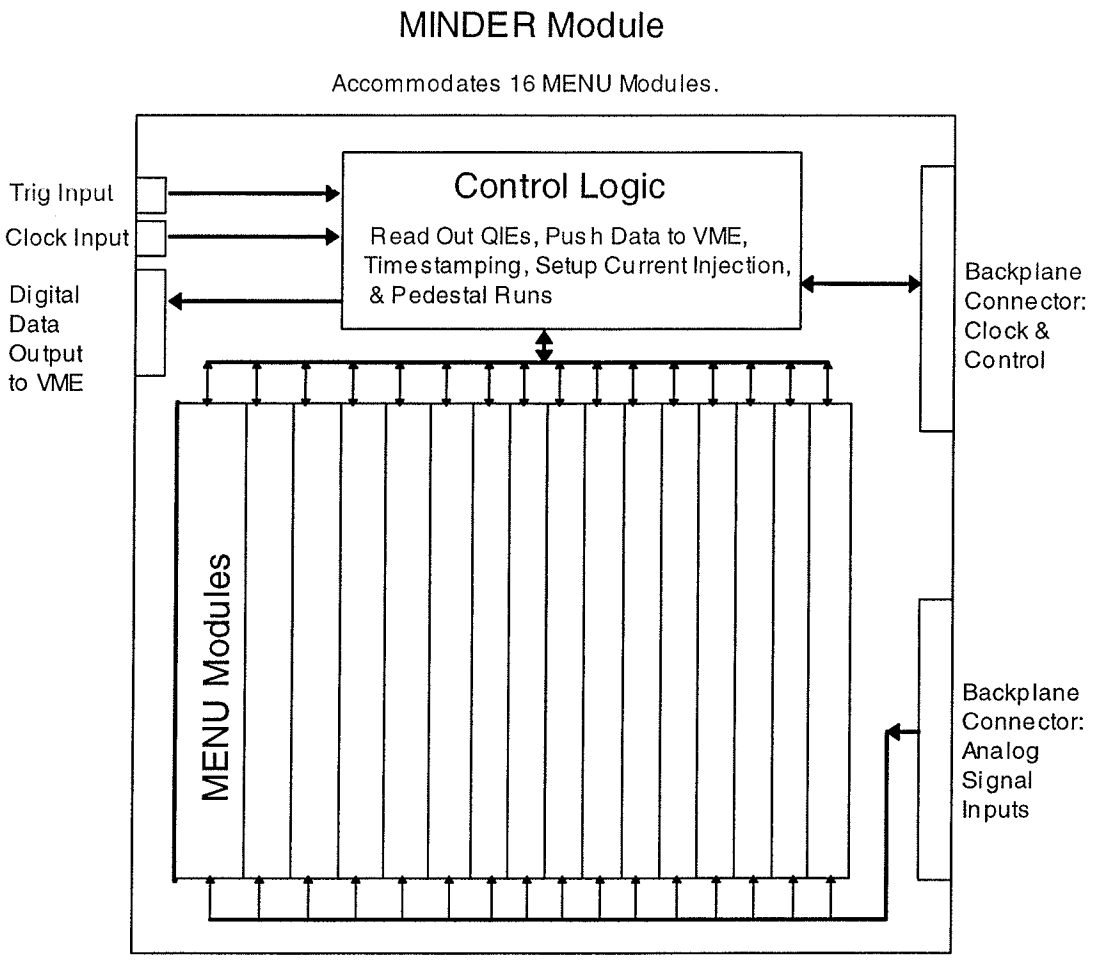

Fig. 10. Block Diagram of MINDER Module

A trigger can occur in one of three ways. In Single Turn Extraction Mode, a signal is received from the Clock Fan-Out Board, indicating that a spill is in progress. This causes the MENU Module to write a continuous data record into its FIFO. The MINDER Module waits until the spill is over before transferring any data from the MENU Modules, at which time the entire contents of all FIFOs are transferred to the VME readout board. In Cosmic Ray Mode and Resonant Extraction Mode, a signal is received from the TRIGGER Module when there is an event of interest. This signal causes the data from several clock cycles to be written into the FIFOs. In Cosmic Ray Mode, the MINDER Module promptly sends FIFO data to the VME MASTER Module, but in Resonant Extraction Mode, FIFO readout is performed after the spill. Lastly, the VME readout board can issue a trigger signal, for use in acquiring pedestals and calibrations. This signal can have a programmable duration, and is controlled by the VME readout board. These modes are described further in Section 5.

All of the MENU Module FIFOs on a given MINDER Module operate synchronously, for all modes of operation. This means that when it is time to transfer data to the VME readout board, all FIFOs contain the same number of data words. (If they do not, then there has been an error, which will be detected.) When data is transferred to the VME readout board, the MINDER Module addresses the first data word in the first MENU Module, then the first data word in the second MENU Module, etc., until all 16 MENU Modules have had one data word read from them. Then, the MINDER Module reads the second data word from each, then the third, etc., until all FIFOs are empty. In this way, the data format and the readout scheme is the same for each mode of operation. The MINDER Module transfers data words to the VME readout board at 33 MHz.

4.4 VME Readout Board

The VME readout board is called the MASTER Module (MINOS Acquisition, Sparsifier, and Time-stamper for Event Readout.) It serves as the interface between the DAQ system and the front end electronics. It resides in a 9U VME crate, and can be far from the photodetectors. It has three primary functions: (1) it provides control signals to the MINDER Crate; (2) it acts as a data funnel, receiving digitized data from the front ends; (3) it processes the data from the MINDER Modules, preparing it for readout by the VME crate computer. The design will be based on the SMXR Module used in the CDF Upgrade [4]. A MASTER Module can service up to 8 MINDER Modules, and each input channel can process data independently.

When the MASTER Module receives data from the MINDER Modules, the data always comes with the same format. A dedicated bit in the data format called the Header Bit, serves as a marker, telling the MASTER Module where the start of the data record is. It is asserted by the MINDER Module on the first word transferred, which is a header word, and is then de-asserted for the duration of the data transfer. Another dedicated bit, called the End of Record (EOR), informs the MASTER Module when the last data word has been received. It is asserted by the MINDER Module on the last data word in a record.

The data is transferred to the MASTER Module by the MINDER Modules, and is written into a FIFO. The MASTER polls the FIFO Empty Flag, looking for data. When data is received, the MASTER begins to read data from the FIFO, looking for the Header Bit. When the MASTER finds a Header Bit, it begins processing the data.

The first two data words are header words. They contain the time-stamp for the data that follows. The MASTER takes these two words and converts the Grey-coded number into a straight binary representation. The 16 QIE data words that follow are associated with this time-stamp. Any data over threshold in the first data set would have this time-stamp appended to it. The next set of 16 words requires the time-stamp to be incremented by one. The MASTER counts data words, and increments the time-stamp counter by one when a new data set is encountered (on every 16th word.) The counting of data words is also used to form a local channel ID.

As QIE data is read, it is processed by the MASTER. The first function is to convert the floating-point QIE data to a linear, 16-bit form. The MASTER uses a look-up table (LUT) to accomplish this. The QIE data word (CAPID, Range Bits, and ADC Bits,) along with the channel ID, form an address into the LUT. The LUT is loaded with values in advance of data acquisition. The value in each location represents the linear, 16-bit data word associated with that QIE data word that points to it. The values are loaded by the VME computer, as a result of a calibration procedure described later. Each LUT handles the 16 channels associated with that input data channel (i.e. a MINDER Module.) The size of the address space is:

(256 ADC codes) * (8 ranges) * (4 CAPIDs) * (16 channels) = 131,072 (17 bits)

After the data is linearized, the MASTER applies a digital threshold to the result. It passes the data that is over threshold, and concatenates the value of time-stamp counter and the channel ID. The new data words are then put into one of two buffers, which can be accessed by the VME computer. One buffer is active for writing data making the other available for reading by the VME computer.

There are 8 types of operation in the MASTER, as shown below. The VME computer controls the type of operation by setting bits in a register on the MASTER.

#	Name	Function
0	Standby Mode	Idle State
1	Data Mode	Normal DAQ (Physics)
2	Calibration	Perform Calibrations
3	Flash Mode	Save/Recall Look-Up Tables
4	VME Mode	Perform VME I/O
5	Diagnostic Data Mode	Process Programmable Normal Data
6	Diagnostic Calibration Mode	Process Programmable CAL Data
7	LUT Diagnostic Mode	Look-Up Table Diagnostics

The MINDER Crate has a simple controller in it called the KEEPER (Krate Electronics Port for Event Readout.) The KEEPER is controlled by the MASTER. The MASTER and KEEPER modules communicate via a simple data link. Through this link, the MASTER can initiate and control DC Current calibrations, enable radioactive source measurement circuitry, and initiate pedestal runs. These operations are also controlled by the VME computer, by setting bits in a register on the MASTER.

4.5 Interface to the DAQ System & Trigger Farm

The interface to the DAQ system is provided by the VME computer, which resides in the 9U VME crate. The computer will operate under VxWorks, and is programmed to perform DAQ and calibrations. This computer can access registers on the MASTER Module, and thereby control the acquisition of event data, pedestals, and calibration data. The computer also controls the writing of data into the look-up tables on the MASTER Module. The MASTER Module is compliant with VME-64 protocol.

As data is acquired in the MASTER Module, it is put into one of two buffers on the module. The VME computer controls which of the buffers is active for writing. There is a timing signal on the VME backplane, supplied by the Clock System. At specified intervals, the signal is sent to the VME computer, which signals that it is time to read a buffer. The VME computer in turn sends a command onto the backplane, changing the active buffer number on the MASTER Module. The VME computer is then free to read out the contents of the inactive buffer. In this way, time blocks of data are formed, making it easier for the VME computer to time-order the data.

An important function of the VME computer is to process calibration data, and calculate the values to load into the look-up tables on the MASTER Module. CDF used this technique, with a module very similar to the MASTER Module. Much of the experience from this effort will be useful in writing these programs for MINOS.

4.6 Triggering

A separate board will be provided for triggering on cosmic rays. This board resides in the MINDER Crate, and receives signals from all the dynodes of the photodetectors associated with that crate. The board contains discriminators with separate programmable thresholds. When a photodetector receives a signal from a cosmic ray, the discriminator for that photodetector fires, and this triggers the acquisition of QIE data on the MENU Module associated with that detector.

In the simplest implementation, the signal from each discriminator is sent directly to the associated MINDER Module, which causes QIE data to be saved in the FIFOs on the MENU Module. Each discriminator would have a point-to-point connection to the MINDER. Other, more sophisticated triggers, are possible with this implementation, since all of the discriminators are on the same board. Since the dynode signals have approximately a factor of 3 less gain, it is advantageous that they be off the MINDER Modules, to reduce noise pickup from digital activity.

4.7 System Timing

There are two components to the Clock System on the Near Detector. The first is the Master Clock Module, which receives the RF clock from the Main Injector, and fans it out to every Front End Crate. The Master Clock provides two other signals. It broadcasts a reset for the time-stamp counters on the MINDER Modules, once per second. It also sends out a signal indicating that a spill is in progress. Both of these signals must be timed precisely with the RF clock, to avoid time-stamp problems in the front end modules. This module is similar to that built for the CDF and D0 Upgrades [5].

The second component is the Clock fan-Out Module. This board resides in the Front End Crates. It receives the timing signals from the Master Clock, and in turn fans them out to each MINDER Module. The fan-out will be implemented using point-to-point connections to reduce clock skew and other loading problems. This module is also similar to one built for CDF [5].

5. Modes of Operation

5.1 Single Turn Extraction Mode

In Single Turn Extraction Mode, the front end electronics digitizes and records on every RF clock cycle. A signal is sent to every MINDER Module from the Clock System, indicating that a spill is in progress. The MINDER in turn sends an enable to the MENU Modules, which allows QIE data to be written into the FIFOs. The leading edge of the spill marker also causes the value of the time-stamp to be recorded in a register on the MINDER Module, to become part of the header words for that data record. The QIE data is written into the FIFOs on the MENU Modules on every RF clock. This continues until the spill-in-progress signal is de-asserted by the Clock System, which causes the writing of data into the FIFOs to halt.

When the spill is over, the MINDER begins the readout operation. First the MINDER sends out the time-stamp as the first two data words. It also asserts the Header Bit on the first word, indicating a start of data record. The MINDER then starts up an on-board sequencer, which addresses each MENU Module, one at a time, reads a single data word from the FIFO, and sends it to the MASTER. The MINDER continues on to the next channel, sending the first data word from the FIFO, and on through the 16th channel. The MINDER then starts over, reading the second word from all the MENU Modules, etc. The operation continues until all data words are read from the FIFOs. FIFO empty flags from the MENU Modules indicate the state of the FIFOs, and the MINDER monitors them. Note that data acquisition (the writing of new data into the FIFOs) is suspended during this period. On the last data word, the MINDER asserts the EOR bit, indicating that the end of the data record has been reached.

There is dead-time associated with sending data to the MASTER. QIE data words are transferred to the MASTER on a 33 MHz clock. The period that data acquisition is suspended is given by:

(10 uS Spill / 19 nS RF) * (16 Channels) * (33 nS/Word) = ~275 uSec

This dead-time occurs after the spill, so there is no loss of data during the spill. The time between spills is on the order of 1 second, so the dead-time is not an issue for the spill itself.

As data is received by the MASTER, it is processed as described previously: it is sent through the LUT, zero-suppressed, time-stamped, and put into the readout buffer, as controlled by the VME computer. The MASTER stops processing data when it encounters the EOR bit in the last data word. It then reverts to a polling mode, where it looks for new data to come in from the MINDER Module.

5.2 Cosmic Ray Mode

In between spills, the front end electronics will run in Cosmic Ray Mode. In this mode, the electronics digitizes and records data only when a trigger signal is generated by the dynode discriminator on the TRIGGER Module. The RF clock continues even between spills, so that the QIEs digitize continuously. When a cosmic ray event occurs, the dynode discriminator fires, and a signal is sent to the associated MINDER Module. This causes the MINDER to write the value of the time-stamp counter into a register, to become part of the header word for this data record. The MINDER also sends a signal to the MENU Modules, allowing QIE data to be written into the FIFOs. All MENU Modules on that particular MINDER Module respond synchronously to this signal. The FIFO write enable is arranged to span over 8 RF clock cycles, so that late signals from the scintillator can be acquired and digitized. Note that there is an inherent delay in the QIE as to when the digitized data is available from an event. It takes several clock cycles to get a data word from the QIE. The dynode discriminator is fast enough, and the transmission path short enough, so that there is no problem in asserting the trigger signal at the MENU Module in time to capture the primary event.

After the last data word is stored in the FIFO, the MINDER begins sending data to the MASTER, in the same way as in Spill Mode. The MINDER sends out the time-stamp in the first two words, and asserts the Header Bit on the first word. The MINDER then starts up the on-board sequencer, reading the first data word from all channels first, then the next data word, and on, until all the FIFO empty flags are set. The MINDER checks the FIFO empty flags from the MENU Modules to determine when the last data word has been sent. Again, the data acquisition is again suspended during this period. The dead-time associated with sending data to the MASTER is given by:

(8 data words/channel) * (16 Channels) * (33 nS/Word) = ~4.5 uSec

As data is received by the MASTER, it is processed in the same way as in Spill Mode. The only difference is that the data record for Cosmic Ray Mode is significantly shorter. As before, the MASTER looks for the EOR bit on the last data word, to indicate when the end of record has been reached.

5.3 Resonant Extraction Mode

In Resonant Extraction Mode, data collection is triggered, as in Cosmic Ray Mode, but FIFO readout is deferred until the spill is over. So long as no FIFOs overflow, there is no dead-time during the spill.

5.4 Pedestal Mode

The MASTER Module can force writing of data into the FIFOs on the MENU Modules. The VME computer sets a bit in a control register on the MASTER Module. This causes a command to be sent from the MASTER Module to the KEEPER, setting up the Pedestal Mode. The KEEPER transmits this signal across the backplane of the Front End Crate, which is received by all the MINDER Modules in the crate. When the MINDER Module receives this signal, it generates a signal that causes QIE data to be written into the FIFOs. This also causes the acquisition of the time-stamp value from the counter, as before. The signal is asserted for a prescribed amount of time, enough to acquire many pedestal events in the FIFOs. At the end of the acquisition period, the MINDER sends data to the MASTER in the same way as described previously. The MASTER reads the data, processes it, and then can be programmed to repeat the operation.

5.5 DC Current Calibration Mode

Calibration Mode is similar to Pedestal Mode. The data is acquired in the same way. The primary difference is that the MASTER must also enable the DC Current Injection Circuitry on the MENU Modules. This is done by setting a calibration enable bit in a register on the MASTER, which in turn is sent to the MINDER Modules through communication with the KEEPER. In addition, the MASTER must also control the DAC on the KEEPER. This is all done under program control through the VME computer.

In Calibration Mode, the DAC is swept through a range of values, enough to acquire several data points on each QIE range. Because the QIE response is piecewise-linear with larger slopes on the low end of the scale, the settings of the DAC must be tailored accordingly. Experience has shown that about 10 points on each range are all that is needed to get a good fit in calculating slopes and offsets.

For each DAC setting, data is acquired by the MASTER. In this mode the MASTER writes the raw QIE data directly into the readout buffer, bypassing the LUT. The VME computer reads this data, calculates averages for each CAPID for each channel, and stores the result in local memory. The program continues until the DAC has been swept through the entire range. The VME computer then calculates the fits. This produces the 64 calibration constants for each channel. These constants can be read out by the DAQ system and stored in a database to monitor the quality of the system.

The next step is for the VME computer to calculate the values to be loaded into the LUTs. When this is done, and the values loaded, a command can be issued to the MASTER, causing the values of the LUTs to be saved in Flash Memory. In so doing, power can be removed from the crate without the need to reload the LUT. Upon power-up, the MASTER automatically loads all LUTs from Flash memory.

5.6 Radioactive Source Monitoring Mode

This mode operates the same as pedestal Mode. In this case, the MASTER causes the source monitoring circuitry to be enabled. The data is then acquired as described previously.

6. Implementation and Physical Layout

6.1 Front End Crates

The front end crates will be 6U Euro-style crates. They must be mounted close to the photodetectors to keep the signal cables between the photodetectors and the electronics as short as possible. Possible layout schemes are shown in Fig. 11.

The crates will be purchased as a commercial product. 6U crates are readily available and are inexpensive. The backplane could be a VME backplane, but the crate will not be operated as a VME crate. The instrumentation in the crate does not require a high level of digital communication, so the VME protocol is not needed

6.2 PMT Signal Cables

The signal cables between the photodetectors and the MINDER Crate must be kept short, preferably less than 1 meter. In addition, the cables must be shielded to avoid noise pickup. It is planned to use coaxial ribbon cable, RG174 or better. The cables will connect onto the dark box, and also onto an Auxiliary (AUX) Board, which in turn plugs into the rear of the MINDER Crate. The AUX Board has no active circuitry, and only acts as strain relief for the signal cables.

6.3 Power and Cooling

The MINDER Crates will use linear, 60 Hz supplies. The power supplies may need to be specified as a custom unit, but can be built commercially. The load is estimated to be approximately 500 Watts per crate.

The VME crates can use switching supplies. These can be purchased as a commercial product. The load is estimated to be approximately 500 Watts per crate.

The MINDER Crates will be cooled using chilled water. This is needed because of the close proximity of the electronics to the photodetectors. The gain and noise of the photodetectors are very sensitive to heating, and the QIE electronics are not low power. The water cooling will help reduce the heating of the photodetectors by the electronics.

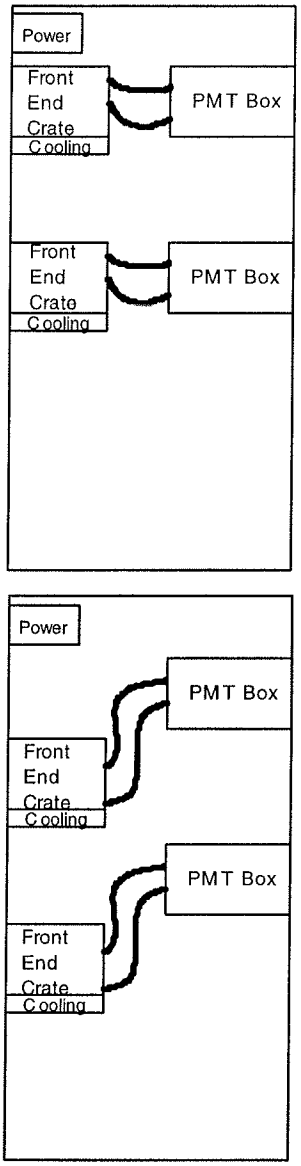

Fig. 11 Two Possible Rack Layout Configurations
(Side View)

6.4 VME Readout Crates

The VME Crates will be standard, and purchased as a commercial product.

7. Bibliography

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Specifications for the MINOS MINDER Crate Backplane

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Preliminary

I. Introduction

This document describes the signals and the pin-out of the MINDER backplane. The J1 provides the digital signals needed to communicate between the MINDER and the KEEPER. The J2 provides signal feed-throughs for the phototube signals, in the signal transmission between the Auxilary cards in the rear of the crate, and the MINDERs (and KEEPER.) The J2 also distributes the power needed for the analog voltages.

II. J1 Backplane

1. Addressing: 12 bits

   MADD[11:0]

   Each Module shall have a set of 5 switches that sets it's slot address in the MINDER Crate. The slot address shall map into address space. (The slot address shall also determine which of the primary trigger signals a card responds to.) The address lines are sourced by the KEEPER.

2. Data: 16 bits

   MDATA[15:0]

   Used for general purpose I/O. The data lines on the backplane are bi-directional.

3. Data Strobes: 2 bits

   MSTB[1:0]

   Essentially 1 signal, OR'ed together on each card. Follows standard VME protocol. The signals are sourced by the KEEPER.

4. Data Bus Direction: 1 bit

   MWRITE*

   Determines the state of the data bus on the backplane. It is low-asserted (LOW = WRITE by KEEPER, HIGH = READ by KEEPER.) The signals are sourced by KEEPER.

5. Data Acknowledge: 1 bit

   MDTACK*

   This is the handshake between a MINDER and the KEEPER that a data transfer has been completed. It is low-asserted. The signal is sourced by the MINDERs using open collector outputs, and is wire-OR'ed on the KEEPER.

II. J1 Backplane (continued)

6. Address Enable: 1 bit

   MENBL*

   This is the enable to allow a card to be addressed. The signal is sourced by the KEEPER, and is low-asserted.

7. Crate-wide Reset: 1 bit

   MRESET*

   Used to reset certain registers on all MINDER Modules in the crate simultaneously (to be defined.) It is low-asserted. The signal is sourced by the KEEPER.

8. Control Bits: 8 bits

   MCTRL*[7:0]

   These are control lines used to set up conditions on all MINDER Modules in the crate simultaneously. (The functions are to be defined. Functions include normal data taking, current calibration, diagnostic data, etc.) The signals are sourced by the KEEPER, and are low-asserted.

9. Status Bits: 4 bit

   MSTAT*[3:0]

   These are status lines used to detect errors on the MINDER Modules. The signal MSTAT0* is reserved for use by the MINDER Timing Module (MTM.) The signals MSTAT1*, MSTAT2*, and MSTAT3* are for use by the MINDER Modules. (The functions are to be defined. Functions include transmission errors, clock sync errors, etc.) They are low-asserted. The signal are sourced by the MINDERs using open collector outputs, and are wire-OR'ed on the KEEPER. The KEEPER shall send MSTAT0* to the MASTER on a dedicated signal line. The KEEPER shall AND together MSTAT1*, MSTAT2, and MSTAT3*, and send the result to the MASTER on a dedicated signal line. The MINDERs will have to be queried to find the offending module.

II. J1 Backplane (continued)

10. Trigger Bits: 7 bits

MTRIG*[6:0]

These signals have several functions. MTRIG*[3:0] are the dynode trigger bits. The dynode signals are discriminated by the KEEPER, and the result sent out onto the MINDER backplane on dedicated signal lines. All four signals are received by all MINDER cards in the crate. A given MINDER Module shall be programmed as to which signal to process by the slot that it resides, and the position of it's address switches.

The signals MCTRL*[5:4] are for additional triggering functionality, and are not yet defined. One function shall be a global trigger, which causes all MINDER Modules to acquire data simultaneously, as needed in performing calibrations.

The signal MCTRL6* is reserved for use by the LED flashing system. When a trigger signal is received by the KEEPER, MCTRL6* is asserted after a fixed delay and for a fixed duration. Any dynode trigger generated during this gate shall be marked as a flash event.

The signals are sourced by the KEEPER, and are low-asserted.

11. Power: 3 pins of +5V Digital

Used for digital circuitry only.

12. Digital Ground: 7 pins of Digital Ground

Used for digital circuitry only.

Pin Number	Row A Signal Name	Row B Signal Name	Row C Signal Name
1	MDATA0	X	MDATA8
2	MDATA1	X	MDATA9
3	MDATA2	X	MDATA10
4	MDATA3	X	MDATA11
5	MDATA4	X	MDATA12
6	MDATA5	X	MDATA13
7	MDATA6	X	MDATA14
8	MDATA7	X	MDATA15
9	GND	X	GND
10	X	X	X
11	GND	X	X
12	MSTB1*	MSTAT0*	MRESET*
13	MSTB0*	MSTAT1*	X
14	MWRITE*	MSTAT2*	X
15	GND	MSTAT3*	X
16	MDACK*	X	X
17	GND	X	MCTRL7*
18	MENBL*	X	MCTRL6*
19	GND	X	MCTRL5*
20	X	GND	MCTRL4*
21	X	X	MCTRL3*
22	X	X	MCTRL2*
23	X	GND	MCTRL1*
24	MADD5	MTRIG6*	MCTRL0*
25	MADD4	MTRIG5*	MADD11
26	MADD3	MTRIG4*	MADD10
27	MADD2	MTRIG3*	MADD9
28	MADD1	MTRIG2*	MADD8
29	MADD0	MTRIG1*	MADD7
30	X	MTRIG0*	MADD6
31	X	X	X
32	+5V Digital	+5V Digital	+5V Digital

Table 1. J1/P1 Pin Assignments for the MINOS MINDER Crate Backplane

III. J2 Backplane

1. Power: 6 pins of +3.3V Digital

   VDIG1 is +3.3V

   Used for powering the MENU Modules only!

2. Power: 6 pins of +12V Analog

   VANA4 is +12V

   Used for analog circuitry only.

3. Power: 3 pins of +5V Analog

   VANA3 is +5V

   Used for analog circuitry only.

4. Power: 3 pins of -5V Analog

   VANA2 is -5V

   Used for analog circuitry only.

5. Power: 3 pins of -12V Analog

   VANA1 is -12V

   Used for analog circuitry only.

III. J2 Backplane (continued)

6. Precision Calibration Voltage: 1 pair of pins

   VCAL+, VCAL-

   This is differential calibration voltage used to calibrate the QIEs and trigger discriminators. It is sourced by a DAC on the KEEPER. The signals must be received differentially by all MINDER Modules, using a higg-impedance receiver.

7. PMT Input Signals - 16 pins

   Used to input PMT signals to the MINDER Modules.

8. PMT Return Signals - 37 pins

   Used to return the current pulses from the MENU Modules to the PMTs.

Pin Number	Row A Signal Name	Row B Signal Name	Row C Signal Name
1	AGND	AGND	AGND
2	MVDIG1	MVDIG1	MVDIG1
3	MVDIG1	MVDIG1	MVDIG1
4	AGND	AGND	AGND
5	MVANA4	MVANA4	MVANA4
6	MVANA4	MVANA4	MVANA4
7	AGND	AGND	AGND
8	MVANA3	MVANA3	MVANA3
9	AGND	AGND	AGND
10	MVANA2	MVANA2	MVANA2
11	AGND	AGND	AGND
12	MVANA1	MVANA1	MVANA1
13	AGND	AGND	AGND
14	AGND	VCAL-	AGND
15	RET	VCAL+	RET
16	RET	RET	PMT_SIG0
17	PMT_SIG1	RET	RET
18	RET	RET	PMT_SIG2
19	PMT_SIG3	RET	RET
20	RET	RET	PMT_SIG4
21	PMT_SIG5	RET	RET
22	RET	RET	PMT_SIG6
23	PMT_SIG7	RET	RET
24	RET	RET	PMT_SIG8
25	PMT_SIG9	RET	RET
26	RET	RET	PMT_SIG10
27	PMT_SIG11	RET	RET
28	RET	RET	PMT_SIG12
29	PMT_SIG13	RET	RET
30	RET	RET	PMT_SIG14
31	PMT_SIG15	RET	RET
32	RET	RET	RET

Table 2. J2/P2 Pin Assignments for the MINOS MINDER CrateBackplane