

**Technical Design Specification  
of the  
MASTER Module  
for the  
MINOS Near Detector  
Front End Electronics**

**By**

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## 1. Introduction

There are two primary parts to the front end electronics for the MINOS Near Detector. The front end crates, called MINDER Crates, contain the QIE electronics. The QIEs receive charge signals, digitize them, and store the data in local FIFOs pending readout. When a readout cycle is initiated, the digitized data is sent to VME Readout Crates. They act as a data funnel, collecting fragments of events together for further processing. The data is zero-suppressed and reformatted, and put into holding buffers, where it can be accessed by the VME computer that resides in each crate. The computer, called the ROP (Read Out Processor), collects data from all VME readout boards in the crate, time orders the data, and then sends it to the DAQ system for event building and selection. Refer to [1] for a detailed description of the system.

The VME readout board is called the MASTER Module (MINOS Acquisition, Sparsifier, and Time-stamper for Event Readout.) It serves as the interface between the DAQ system and the front end electronics. It resides in a 9U VME crate, and can be far from the photodetectors. It has three primary functions: (1) it acts as a data funnel, receiving digitized data from the front ends; (2) it processes the data received from the front end, preparing it for readout by the ROP; (3) it provides control signals to the MINDER Crate. The design is based on the SMXR Module used in the CDF Upgrade [2]. A MASTER Module can service up to 8 MINDER Modules, and each input channel can process data independently.

This note describes the technical design specifications of Version 2 of the MASTER Module. Not all of the features described have been implemented in Version 1, although this version is considered obsolete. A description of the VME interface for the MINOS data acquisition system is given in [3].

## 2. General Description

The MASTER Module is designed to read out and support the QIE, a custom integrated circuit designed for high-rate High Energy Physics experiments [4-5]. A special version of the QIE has been developed for MINOS. The QIE resides in the MINDER Crate. It is *dead-timeless* (no dead time associated with digitization), and digitizes at a clock frequency of 53 MHz, which is matched to the RF frequency of the NUMI beamline. Each data word produced by the QIE is called a *timeslice* (TS), because it represents the charge received from the detector during that RF clock cycle. The QIE is mounted on a daughter board called the MENU Module. These boards also contain the ADC, data buffering, and circuitry for performing electronics calibrations. Data is digitized and stored on these modules, and made available for readout when addressed.

The MENU Modules are mounted on a motherboard called the MINDER Module. These boards contain support circuitry for the MENU Modules, including *timestamping* (the formation of a time stamp to indicate the relative time of a data word), and they control the multiplexing of data from each MENU Module during read-out.

When data is ready for readout, it is transmitted from the MINDER Modules to a readout board called the MASTER Module, which resides in a 9U VME crate. The MASTER Module receives data from up to 8 MINDER Modules. The MASTER Module also provides control for the MINDER Crate. There is a simple controller in the MINDER Crate called the KEEPER, which is controlled by the MASTER. One of the functions is to control a DAC that resides on the KEEPER. The DAC is used for calibrating the QIEs. The MASTER also sets up calibration runs, pedestal runs, and other diagnostic functions through communication with the KEEPER.

When the MASTER Module receives data from the MINDER Modules, the data always comes with the same format. A dedicated bit in the data format called the Header Bit, serves as a marker, indicating the beginning of a data record. It is asserted by the MINDER Module on the first word transferred, which is a header word, and is then de-asserted for the duration of the data transfer. Another dedicated bit, called the Trailer Bit, informs the MASTER Module when the last data word has been received. It is asserted by the MINDER Module on the last data word in a record.

The data is transferred to the MASTER Module by the MINDER Modules, and is written into a FIFO. The MASTER polls the FIFO Empty Flag, looking for data. When data is received, the MASTER begins to read data from the FIFO, looking for the Header Bit. When the MASTER finds a Header Bit, it begins processing the data.

The first three words in a transmission cycle are header words. They contain the timestamp for the data that follows. The MASTER takes the header words and converts them into a straight binary representation. The 16 QIE data words that follow are associated with this timestamp. Any data over threshold in the first data set would have this timestamp appended to it. The next set of 16 words requires the timestamp to be incremented by one. The MASTER counts data words, and increments the timestamp

counter by one when a new data set is encountered (on every 16th word.) The counting of data words is also used to form a local channel ID.

As QIE data is read, it is processed by the MASTER. The first function is to convert the floating-point QIE data to a linear, 16-bit form. This is called *linearizing* the data. The MASTER uses a look-up table (LUT) to accomplish this. The QIE data word (CAPID, Range Bits, and ADC Bits,) along with the channel ID, form an address into the LUT. The LUT is loaded with values in advance of data acquisition. The value in each location represents the linear, 16-bit data word associated with that QIE data word that points to it. The values are loaded by the ROP, and are obtained from a special calibration procedure. Each LUT handles the 16 channels associated with that input data channel (i.e. a MINDER Module.) The contents of the LUT can be saved in on-board flash memory, which maintains the contents after power-down. The LUTs are reloaded automatically on power-up, and can be reloaded by a command from the ROP.

After the data is linearized, the MASTER applies a digital threshold to the result. It passes the data that is over threshold, and concatenates the value of timestamp counter and the channel ID. The accepted data words are then written into one of two buffers, which can be accessed by the ROP. One buffer is active for writing data at a given time, making the other available for reading.

The MINDER Crate has a simple controller in it called the KEEPER. A data cable connects it to the J3 connector of the MASTER. Communication between the ROP and the KEEPER is done through VME transactions. The KEEPER has it's own section of VME address space. Through this communication path, the ROP can initiate and control DC Current calibrations, initiate pedestal events, perform diagnostics, and set up conditions for performing data acquisition.

### 3. Technical Specifications

#### 3.1 Operational Modes

3.1.1 The MASTER Module shall have different modes in which it can operate. The modes are shown in the Table 3.1 below.

<u>Mode #</u>	<u>Name</u>	<u>Function</u>
0	Standby Mode	Idle State
1	Data Mode	Normal DAQ (Physics)
2	Calibration Mode	Acquire and Process Calibration Data
3	Flash Mode	Save/Recall Look-Up Tables
4	VME Mode	Perform VME I/O
5	Diagnostic Data Mode	Process Programmable Normal Data
6	Diagnostic Calibration Mode	Process Programmable CAL Data
7	undefined	

**Table 3.1 MASTER Module Operational Modes**

3.1.2 The mode of operation is controlled by setting bits in the Status Register of the MASTER Module. The ROP must select one of the operational modes as part of the setup of the MASTER Module, before an operation begins. See Section 3.12.

3.1.3 Standby Mode is an idle state. In this mode, all processing functions on the MASTER Module are halted.

3.1.4 Data Mode is used for acquiring linearized QIE data from the MINDER Modules. This mode is used for acquiring events from physics. The data processed by the MASTER Module is in 16 bit linear format, and includes a timestamp and channel address. See Section 3.4 for a definition of the format. The data is written to a Readout Buffer, and accessed from VME according to Section 3.7.

3.1.5 Calibration Mode is used for acquiring raw QIE data from the MINDER Modules. This mode is used for acquiring events associated with electronics calibration. The data processed by the MASTER Module is left in the raw, floating-point format as produced by the QIEs. See Section 3.5 for a definition of the format. The data is written to a Readout Buffer, and accessed from VME according to Section 3.7.

### 3.1 Operational Modes (Cont.)

- 3.1.6 Flash Mode is used for accessing (downloading, uploading, and erasing) the flash memory, which is used to store the contents of the look-up tables (LUTs.) See Section 3.9.
- 3.1.7 VME Mode is used to access certain registers on the MASTER Modules. These include the Status Register, accessing the look-up tables, and accessing the Diagnostic Memory. See Section 3.8 and Section 3.12.
- 3.1.8 Diagnostic Data Mode is used for processing pre-programmed data that mimics real QIE data, in the same way that real QIE data is processed in Data Mode. The data processed by the MASTER Module is in 16 bit linear format, and includes a timestamp and channel address.
- 3.1.9 Diagnostic Calibration Mode is for processing pre-programmed data that mimics real QIE data, in the same way that real QIE data is processed in Calibration Mode. The data processed by the MASTER Module is left in the raw, floating-point format as produced by the QIEs.

### 3.2 Data Input from the MINDER Modules

- 3.2.1 The MASTER Module shall be capable of receiving data streams from 8 MINDER Modules.
- 3.2.2 The input channels shall operate independently of one another, in terms of how the data is processed and put into a Readout Buffer.
- 3.2.3 The input connectors are located on the front panel of the MASTER Module.
- 3.2.4 The data transmission from the MINDERs to the MASTER is uni-directional.
- 3.2.5 The logic family used for data transmission is LVDS.
- 3.2.6 Each data input contains 18 differential bits. In general, the bits are defined as:

- 13 Data Bits
- 1 Parity Bit
- 1 Header Bit
- 1 Trailer Bit
- 1 Error Bit
- 1 Data Strobe

- a. The Data Bits are general purpose, and have different meanings, depending on the type of operation. See Section 3.3.
- b. The Parity Bit is used to detect errors in the transfer of data between the MINDER Modules and the MASTER. The parity bit shall generate EVEN Parity (an even number of one's transmitted by the MINDER, including the parity bit.)
- c. The Header Bit is asserted on the first word sent in a data transmission cycle, and then de-asserted.
- d. The Trailer Bit is asserted on the last word sent in a data transmission cycle, and then de-asserted.
- e. The Error Bit is asserted when the data transmission from the MINDER to the MASTER is aborted prematurely. See Section 3.13.
- f. The data strobe is used to strobe the data into the input FIFO on the MASTER Module.

**3.2 Data Input from the MINDER Modules (Cont.)**

3.2.7 The Input Data Connector on the MASTER Module is defined in Appendix I.

**3.3 Format of Data from the MINDER Modules**

3.3.1 The first three words sent in a data transmission sequence contain the timestamp fiducial for that data record. The format is given in Table 3.2.

- a. The total size of the timestamp is 27 bits.
- b. Word 1: includes any header information from the MINDER; also includes the msb of the timestamp (1 bit); also includes 3 bits which indicate the data type (pedestal, calibration, spill, cosmic ray, etc.)
- c. Word 2: timestamp high word (13 data bits)
- d. Word 3: timestamp low word (13 data bits)

Word	Bits: 12 11 10 09 08 07 06	05 04 03	02 01	00
1	Undefined (Set Low)	Data Type	Undefined (Set Low)	Timestamp MSB
2	Timestamp High Word (13 Bits)			
3	Timestamp Low Word (13 Bits)			

**Table 3.2 Timestamp Data Format**

3.3.2 After the timestamp fiducial is sent, the words that follow are raw QIE data. The format is given in Table 3.3. The processing of data is described in Section 3.4 and Section 3.5.

- a. The size of each data word is 13 bits.
- b. The format is defined as:

12 11	10 09 08	07 06 05 04 03 02 01 00
CAPID Bits	Range Bits	QIE ADC Bits

**Table 3.3 QIE Data Format**

**3.3 Format of Data from the MINDER Modules (Cont.)**

3.3.3 The QIE data will be sent to the MASTER in "time-ordered" sequence. Timeslice 0 (TS00) for all channels is sent first, then Timeslice 1 (TS01), etc.:

CH00, TS00

CH01, TS00

CH02, TS00

...

CH15, TS00

CH00, TS01

CH01, TS01

CH02, TS01

...

CH15, TS<sub>nn</sub>

where nn is : ~8 for cosmic ray data

~526 for spill data (single-turn extraction, 10 uSec long  
with a 19 nSec QIE clock)

~8 for spill data (resonant extraction)

~64 for VME Triggers

3.3.4 Data transmission from the MINDER Modules always has the same format as given in Section 3.3.1 and 3.3.2 above, independent of the operational mode of the MASTER Module.

### 3.4 Processing of Data in Data Mode

Data Mode is designed to process events from the detector. Generally, the events are triggered from an external process. Once triggered, data is sent from the front end electronics to the MASTER Module as described in Section 3.2.

3.4.1 Data is received from the MINDER Modules with the format as described in Section 3.3. It is written into an input FIFO, using the data strobe signal that is sent along with the data.

3.4.2 The MASTER Module polls the input FIFO, looking for a word that has the Header Bit set, as specified in Section 3.2. The first word received that has the Header Bit set marks the first word in a data transmission sequence.

3.4.3 The header data is processed as follows:

- a. Form the 27 bit timestamp fiducial, and use for forming timestamps for the QIE data words that pass threshold.
- b. Save the data type bits. They must also be appended to the QIE data.

3.4.4 The timestamps are calculated by the MASTER Module from the timestamp fiducial. They are stored in a holding register, and appended to processed QIE data. The timestamps are formed as follows:

- a. Begin with the timestamp fiducial.
- b. TS00 is associated with the timestamp fiducial.
- c. After 16 QIE words are read, the timestamp value is incremented by 1. This new timestamp is associated with TS01.
- d. Continue incrementing the timestamp value after every 16 QIE data words are read, until all words have been processed.

3.4.5 After the header words have been read, the next words in the input FIFO are QIE data. The QIE data is processed as follows:

- a. Read the first CAPID. Use this as the first CAPID reference.
- b. As each QIE data word is read, check the parity and CAPID. Set an error flag if there is an error. See Section 3.13.

**3.4 Processing of Data in Data Mode (Cont.)**

3.4.5 The QIE data is processed as follows (cont.):

- c. Increment the CAPID reference after every 16 QIE data words have been read, modulo 4.
- d. As each QIE data word is read, linearize each word using the LUT. (See Section 3.9.)
- e. Apply threshold to each linearized data word.
- f. Save any data that passes threshold. Discard those data words that are below threshold.
- g. Append the timestamp, data type, and error bits.
- h. Save the data in active Readout Buffer. See section 3.7.

3.4.6 The format of data saved into the Readout Buffer has the following format:

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
H	ERR[2:0]		GA[4:0]				ICH		CH[4:0]				Linearized ADC Value ADC[15:0]																			
L	DT[2:0]		X	Timestamp TS[26:16] Hi Word												Timestamp TS[15:0] Low Word																

- ERR[2:0] - Error Codes
- GA[4:0] - Geographical Address
- ICH[2:0] - MASTER Module Input Channel (8 total)
- CH[4:0] - MINDER Module Channel Number
- ADC[15:0] - Linearized 16-Bit ADC Word for One Timeslice
- DT[2:0] - Data Type (Used for indicating spill, calibration, etc.)
- X[1:0] - Reserved
- TS[26:0] - 27-Bit Timestamp for One Timeslice

**Table 3.4 Format of Data in Data Mode,  
As Saved in the Readout Buffer**

### 3.4 Processing of Data in Data Mode (Cont.)

- 3.4.7 Processing continues until the MASTER Module detects a Trailer Bit on a data word. This word is the last one in that data transmission sequence. See Section 3.13 for special procedures when an error bit is encountered in the data stream from the MINDER.
- 3.4.8 For each of the types of data acquisition (Single-Turn Spill Mode, Resonant Extraction Spill Mode, and Cosmic Ray Mode), a fixed number of words is sent in each case, but the numbers may be different among the different data types. The MASTER shall be capable of processing the data independent of the actual number of words sent in a given data transmission. The MASTER shall begin a data processing sequence when it receives a Header Bit, and end the data processing sequence when it receives a Trailer Bit, as specified in Section 3.2.
- 3.4.9 As data is written into the Readout Buffer, the Word Count Register for the active buffer is incremented to reflect the number of words written. See Section 3.7.
- 3.4.10 In Data Mode, access of the Readout Buffers is done by an external process running in the VME crate. There is no provision to control which buffer is written to through the ROP. See Section 3.7.
- 3.4.11 In Data Mode, the Word Count Register is automatically initialized to zero as part of the external buffer control. In addition, the Word Count Register is decremented as words are read from the Readout Buffer by the ROP. See Section 3.7.

### 3.5 Processing of Data in Calibration Mode

Calibration Mode is designed to process events that contain calibration data, such as pedestals or current injection into the front end electronics. Generally, the events are triggered by the ROP. Once triggered, data is sent from the front end electronics to the MASTER Module as described in Section 3.2. In particular, this mode is designed to bypass the look-up table, passing the raw data to the Readout Buffer.

- 3.5.1 A calibration event is triggered as described in Section 3.5.8. Data is received from the MINDER Modules with the format as described in Section 3.3. It is strobed into an input FIFO, using the data strobe that is sent along with the data.
- 3.5.2 The MASTER Module polls the input data register, looking for a word that has the Header Bit set, as specified in Section 3.2. The first word received that has the Header Bit set marks the first word in a data transmission sequence.
- 3.5.3 The header data is processed in the same way as for Data Mode, described in Section 3.4.3.
- 3.5.5 The timestamps are formed in the same way as for Data Mode, as described in Section 3.4.4.
- 3.5.5 The QIE data is processed as follows:
  - a. Read the first CAPID. Use this as the first CAPID reference.
  - b. As each QIE data word is read, check the parity and CAPID. Set an error flag if there is an error. See Section 3.13.
  - c. Increment the CAPID reference after every 16 QIE data words have been read, modulo 4.
  - d. Save the raw QIE data in the active buffer. Note that:
    - 1. The data is *not* sent through the LUT.
    - 2. The data does *not* have a threshold applied to it.

**3.5 Processing of Data in Calibration Mode (Cont.)**

3.5.6 The format of data saved into the Readout Buffer has the following format. Note that the data is 64 bits, as in Data Mode:

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
H	ERR[2:0]			GA[4:0]				ICH		CH[4:0]				Not Used		CAPID		RANGE		QIE ADC QADC[7:0]												
L	DT[2:0]			X	Timestamp TS[26:16] Hi Word											Timestamp TS[15:0] Low Word																

- ERR[2:0] - Error Codes
- GA[4:0] - Geographical Address
- ICH[2:0] - MASTER Module Input Channel (8 total)
- CH[4:0] - MINDER Module Channel Number
- NotUsed[2:0] - Set Low
- CAPID[1:0] - QIE CAP ID Bits
- RANGE[2:0] - QIE Range Bits
- QADC[7:0] - 8-Bit QIE ADC Word for One Timeslice
- DT[2:0] - Data Type (Used for indicating spill, calibration, etc.)
- X - Reserved
- TS[26:0] - 32-Bit Timestamp for One Timeslice

**Table 3.5 Format of Data in Calibration Mode, As Saved in the Readout Buffer**

- 3.5.7 Processing continues until the MASTER Module detects a Trailer Bit on a data word. This word is the last one in that data transmission sequence.
- 3.5.8 A calibration event is triggered by the ROP by writing to one of two VME memory locations, as described in Appendix VI. Writing to one address causes the event to be triggered, and directs the incoming data to be written to Readout Buffer 0. Writing to the other address causes the event to be triggered, and directs the data to be written to Readout Buffer 1. Note that in Calibrate Mode, the control of the Readout Buffers is *not* done by an external process, as is the case for Data Mode.
- 3.5.9 As data is written into the Readout Buffer, the Word Count Register for the active buffer is incremented to reflect the number of words written. See Section 3.7.

### 3.5 Processing of Data in Calibration Mode (Cont.)

- 3.5.10 In Calibration Mode, the Word Count Register is automatically initialized to zero when the trigger is issued, as described in Section 3.5.8. In addition, the Word Count Register is decremented as words are read from the Readout Buffer by the ROP, as is the case for Data Mode. See Section 3.7. Consequently, the Readout Buffer can hold only one calibration data event per trigger.
- 3.5.11 There is no status bit to indicate when a calibration event is done being processed by the MASTER Module. The preferred method is to poll the Word Count Register to determine when the expected number of words has been written to the Readout Buffer. See Section 3.7, Appendices IV-V, and Appendix VI.

### 3.6 Processing of Data in the Diagnostic Modes

Diagnostic Mode is designed to process pre-programmed events, in order to test the functionality of the MASTER circuitry. Generally, the data may have any form, including test patterns, simulated pedestal or calibration events, or simulated data. In particular, it is not possible for the ROP to write directly to the Readout Buffers from VME. The diagnostic modes must be used to test and diagnose problems with the Readout Buffers. There are two diagnostic modes. In Diagnostic Data Mode, the data is processed as in Data Mode, where the LUT is used. See Section 3.4. In Diagnostic Calibration Mode, the data is processed as in Calibration Mode, where the LUT is bypassed. See Section 3.5. Diagnostic events are triggered by the ROP.

- 3.6.1 In Diagnostic Data Mode and Diagnostic Calibration Mode, pre-determined test data is down-loaded to a diagnostic memory on the MASTER Module.
- 3.6.2 When a diagnostic event is initiated, the data from the diagnostic memory is sent to the data input channels of the MASTER Module. It is received in the same fashion as that from the MINDER Modules, except that the diagnostic data does not go through the data buffers that receive the data from the Data Input Connector.
- 3.6.3 When a diagnostic event is initiated, the data from the diagnostic memory is sent to all input channels. This means that each input processes the same diagnostic data at the same time.
- 3.6.4 In Diagnostic Data Mode, data is processed in the same manner as real data in Data Mode (see Section 3.4.) In Diagnostic Calibration Mode, data is processed in the same manner as real data in Calibration Mode (see Section 3.5.)
- 3.6.5 In Diagnostic Data Mode and Diagnostic Calibration Mode, an event is triggered by the ROP by writing to one of two VME memory locations, as described in Section 3.6.15 and Appendices IV-V. Writing to one address causes the event to be triggered, and directs the incoming data to be written to Readout Buffer 0. Writing to the other address causes the event to be triggered, and directs the data to be written to Readout Buffer 1. Note that in these modes, the control of the Readout Buffers is *not* done by an external process, as is the case for Data Mode.
- 3.6.6 As data is written into the Readout Buffer, the Word Count Register for the active buffer is incremented to reflect the number of words written. See Section 3.7.

**3.6 Processing of Data in the Diagnostic Modes (Cont.)**

- 3.6.7 In the diagnostic modes, the Word Count Register is automatically initialized to zero when the command to initiate a diagnostic event is issued. In addition, the Word Count Register is decremented as words are read from the Readout Buffer by the ROP. See Section 3.7. Consequently, the Readout Buffer can hold only one diagnostic data event per trigger.
- 3.6.8 The Status Register contains a status bit that indicates when a diagnostic event is being processed. See Section 3.12 and Appendices IV-V. The bit is set to a logic 1 while the processing is in progress, and is set to a logic 0 when the processing is completed.
- 3.6.9 The format of the data as written into the Diagnostic Memory is given in Table 3.6. Note that the data is loaded into the Diagnostic Memory using 64-bit block transfers, but only the lower 16 bits of each word is used.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Not Used																E	T	H	P	CAPID	RANGE	QIE ADC	QADC[7:0]								

- E - Error Bit (Premature Termination of Transmission)
- T - Trailer Bit
- H - Header Bit
- P - Parity Bit
- CAPID[1:0] - QIE CAP ID Bits
- RANGE[2:0] - QIE Range Bits
- QADC[7:0] - 8-Bit QIE ADC Word for One Timeslice

Note: The Diagnostic Memory is loaded using 64-bit transfers. Bits 32-63 of the long word are not used.

**Table 3.6 Format of Data as Written into the Diagnostic Memory for use in Diagnostic Data Mode and Diagnostic Calibration Mode**

### 3.6 Processing of Data in the Diagnostic Modes (Cont.)

- 3.6.10 The diagnostic data does not need to have a particular format. However, in order to prevent the MASTER from generating errors, it must obey the data processing rules that apply to the QIE data from the MINDER Modules. In particular:
- a. The CAPID Bits must be arranged so that the first 16 data words have the same value of CAPID. The next value of the CAPID must be incremented by 1, modulo 4, and all of the next 16 data words must have that value. This pattern must continue through the entire set of diagnostic data. If this is not done, an error will be generated (see Section 3.13).
  - b. The number of data words (not counting the 3 Header Words) must be a multiple of 16. If this is not done, an error will be generated. See Section 3.13. An exception is if the Error Bit is also set on the last word, along with the Trailer Bit. See Section 3.13.
  - c. The user must generate the proper value of the Parity Bit. See Section 3.2.6. If this is not done, an error will be generated. See Section 3.13.
- 3.6.11 In the case where the diagnostic data does not mimic QIE data properly, the MASTER shall generate errors when the integrity of the data is incorrect. This includes the proper formation of CAPID Bits and Parity Bit, and the proper word count (modulo 16.)
- 3.6.12 The Diagnostic Memory occupies 256 K Words of memory space (2 MB of address space), where a word is defined as in Table 3.6. See Appendices IV-V for the memory map. The data for a diagnostic event may use any portion of this memory space. However, under certain conditions, it is possible to generate a Buffer Word Count Error if the number of data words processed exceeds the buffer size. See Sections 3.7 and 3.13.
- 3.6.13 The starting point for a diagnostic event can be anywhere in the Diagnostic Memory. The starting address is loaded into a register on the MASTER Module prior to initiating the event. See Appendices IV-V.
- 3.6.14 Data is read from a Readout Buffer by the ROP using extended, non-privileged 64-bit block transfers. See Section 3.8.

**3.6 Processing of Data in the Diagnostic Modes (Cont.)**

3.6.15 A diagnostic event is initiated as follows:

- a. Load Diagnostic Memory with data. The Header Bit does not need to be set on the first word, as this is internally generated in the diagnostic modes. The Trailer Bit *does* need to be set on the last data word. The Parity Bit and CAPID Bits must also be set properly on each data word to avoid generating errors. The loading of the Diagnostic memory is done in VME Mode (see Section 3.1.) The data is loaded as 64-bit words, but only the lower 16 bits is used, as indicated in Table 3.6.
- b. Select the starting address for the diagnostic data. Write the address to the Diagnostic Memory Starting Address (DMSA) Register. See Appendices IV-V for the memory map. The loading of the DMSA Register is done in VME Mode (see Section 3.1.)
- c. Select a Data Type and a Timestamp for the diagnostic event. These should mimic those generated by the MINDER Modules. (The 3 bits of Data Type are generated by the MINDER Modules in normal operation. They are not defined here, and the MASTER Module does not act on them.) The Timestamp is a 27 bit binary number.
- d. Select a Readout Buffer (0 or 1) into which the diagnostic data is to be processed.
- e. Switch to one of the diagnostic modes, as indicated in Table 3.1. The MASTER must be in one of the diagnostic modes to process a diagnostic event.
- f. Write the Timestamp and the Data Type to the Start Diagnostic Data 0 (SDD0) Register to begin a diagnostic event for Readout Buffer 0; write the Timestamp and data Type to the Start Diagnostic Data 1 (SDD1) Register to begin a diagnostic event for Readout Buffer 1. See Appendices IV-V for the memory map. The format is given in Table 3.7.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DT[2:0]			Unused			Timestamp[26:0]																									

TS[26:0] - 27-Bit Timestamp for One Timeslice

DT[2:0] - Data Type (Used for indicating spill, calibration, etc.)

**Table 3.7 Format of Data as Written to Start Diagnostic Data Registers**

### 3.6 Processing of Data in the Diagnostic Modes (Cont.)

#### 3.6.15 Initiating a diagnostic event (cont.):

- g. The loading of the SDD0 or SDD1 Registers is done in Diagnostic Mode (see Section 3.1.) The act of writing to either of these registers starts the processing of a diagnostic event. The Header Bit is automatically generated in this process.
- h. Once either the SDD0 or SDD1 registers are loaded, the MASTER sets bit D7 of the Status register to logic 1, indicating that the processing of a diagnostic event has begun. The MASTER also initializes the Word Count Register to 0.
- i. The processing of diagnostic data continues until a Trailer Bit is encountered in a data word. As data words are written into a Readout Buffer, the Word Count register is incremented. Note that the Master Module will generate an error if no Trailer Bit is encountered.
- j. When a Trailer Bit is encountered, the MASTER sets bit D7 of the Status Register to logic 0, indicating that the processing of the diagnostic event has finished.

### 3.7 Readout Buffers

- 3.7.1 There are two Readout Buffers on each MASTER Module. In Data Mode, while one buffer is active for writing new data, the other buffer is made available to the ROP for reading data previously acquired. (In Calibration Mode and the diagnostic modes, generally the process is such that a selected buffer is written to and then read when the process is over.)
- 3.7.2 The Readout Buffers must be capable of having data from the MINDER Modules written to them, as received from the Data Input Connector. The Readout Buffers must also be capable of having diagnostic data written to them. See Section 3.6.
- 3.7.3 In Calibration Mode, the Readout Buffer to be written is selected when the trigger is generated. See Section 3.5. Only one of the two buffers may be written at a given time. Each MASTER in a VME Crate is operated independently of any others that reside in the crate.
- 3.7.4 In Diagnostic Data Mode and Diagnostic Calibration Mode, the Readout Buffer to be written to is selected when the trigger is generated. See Section 3.6. Only one of the two buffers may be written to at a given time. Each MASTER in a VME Crate is operated independently of any others that reside in the crate.
- 3.7.5 In Data Mode, only one buffer of the two buffers may be written to at a given time. An external process controls the state of the buffers:
- a. A special timing module that resides in the VME Crate called the VME Timing Module (VTM), implements the control of the Readout Buffers. This module receives a programmable Time Block Marker signal from the Master Clock System in the Near Detector, and uses it to generate VME Interrupt Requests. The Interrupt Requests are sent across the backplane of the VME crate. The MASTER Modules in the crate "spy" on the Interrupt signals, and use them to change state of the buffers. The ROP also receives the Interrupts, and uses them to initiate a new cycle for reading data from the buffers. The MASTER Module does not generate Interrupt Vectors in response to these two Interrupt Requests.
  - b. The VTM shall use two VME Interrupt Requests, one for each buffer. IRQ3 shall be associated with the reading Buffer 0. IRQ4 shall be associated with reading buffer 1.

### 3.7 Readout Buffers (Cont.)

#### 3.7.5 Control of buffers in Data Mode (cont.):

- c. Each Interrupt Request shall be asserted in alternating fashion, for example: first IRQ3, then IRQ4, then IRQ3, etc. In this way, a particular Readout Buffer, along with its VME address space, is associated with a particular Interrupt signal.
- d. The convention shall be that the assertion of a particular Interrupt Request causes the associated buffer to be put into the "Read" state, with the other buffer put into the "Write" state
- e. Each MASTER Module handles the control of its own buffers based on this convention. The VME Crate can contain a number of MASTER Modules, and if all are set to Data Mode, the buffers on all MASTERS will change state at the same time. Furthermore, since the Time Block Marker from the Master Clock is sent to all crates in the system, the change in state of the Readout Buffers is synchronized across the entire readout system as well.
- f. When the MASTER Module receives a new IRQ, it generally must change the state of the buffers immediately. If data processing is in progress on a given input channel, the MASTER Module is allowed to finish that processing on that input channel before changing the buffer state for that input channel. However, the buffers for all other input channels not processing data at the time that the new IRQ is received shall change state immediately.
- g. The counter for the Buffer Word Count Register shall be initialized to 0 when a new buffer is placed into the WRITE state.

3.7.6 The two Readout Buffers on each MASTER Module shall be located at different logical VME addresses. The buffer state shall be synchronized across the entire crate, so that the ROP knows where in address space to read the data for a given Time Block period. See Appendices IV-V for a definition of the memory map.

3.7.7 The buffers on the MASTER Module may be configured as separate sections, one for each input channel. However, the readout of the buffer must be such that the data from the different input channels appear contiguously in memory, without gaps in address space.

**3.7 Readout Buffers (Cont.)**

3.7.8 The depth of each Readout Buffer shall be 128K, 64-bit words. This is divided into eight buffers, one for each input channel, where each buffer contains 16K, 64-bit) words.

In normal data taking, only the data greater than or equal to the programmed threshold shall be saved in the Readout Buffers. However, it is desirable to provide the capability to store the data from every timeslice for every channel for the data from a spill. (This can be achieved by setting the threshold to 0.) This provides the ability to debug data transmission and processing problems. To accommodate this operation, the depth of each Readout Buffer shall be:

For Each Input Channel:

$$\begin{aligned}
 16 \text{ Ch/MINDER} * 526 \text{ Timeslices} &= 8,416 \text{ Long Words / MINDER} \\
 &= 67,328 \text{ Bytes / MINDER} \\
 &= 8,416 \text{ Long Words / MINDER} \\
 &> 8\text{K Long Words}
 \end{aligned}$$

For the Entire MASTER Module:

$$\begin{aligned}
 32 \text{ Ch/MINDER} * 526 \text{ Timeslices} * 8 \text{ MINDERS} & \\
 &= 67,328 \text{ Long Words / MASTER} \\
 &= 538,624 \text{ Bytes / MASTER} \\
 &= 67,328 \text{ Long Words / MASTER} \\
 &> 64\text{K Long Words}
 \end{aligned}$$

In order to ensure that the raw data from an entire spill can be recorded, the size of each Readout Buffer on the MASTER Module shall be 128K long words. The size of the buffers for each input channel then corresponds to 16K long words.

### 3.7 Readout Buffers (Cont.)

- 3.7.9 The MASTER Module must make available to the processor the total number of words that are available for reading in a buffer. A register on the MASTER Module, called the Buffer Word Count Register, shall be defined for this purpose. The MASTER Module also contains a register for each channel that contains the number of words written into the buffer for that channel. See Appendices IV-V for the memory map.
- 3.7.10 If a Readout Buffer ever fills completely, the MASTER shall set the word count error bit on the last data word written to the buffer. See Section 3.13.
- 3.7.11 As data words are read from a Readout Buffer by a ROP, the MASTER Module shall decrement the Buffer Word Count Register.
- 3.7.12 The Readout Buffers are READ ONLY from VME. They cannot be written directly from VME.
- 3.7.13 Data is read from a Readout Buffer by the ROP using extended, non-privileged 64-bit block transfers. See Section 3.8.

### 3.8 VME Interface

- 3.8.1 The MASTER Module shall support VME64X specifications, as given in [6-9].
- 3.8.2 The VME base address shall be configured through the use of Geographical Address pins GA4-GA0 from the VME backplane, as specified in the VME64X specifications.
- 3.8.3 The addressing modes that are supported by the MASTER Module are:
- a. Extended non-privileged 64-bit block transfer  
(64-bit data, 32-bit address block transfers)  
Address Modifier: 08
  - b. Extended non-privileged data access  
(32-bit data, 32-bit address single transfers)  
Address Modifier: 09
- 3.8.4 The MASTER Module shall support block transfers of data. The VME64 spec specifies 256 8-byte transfers in block transfer mode as the maximum size. The VME interface on the MASTER Module shall abide by this specification. If data blocks are larger than this, then multiple block transfer cycles must be performed.
- 3.8.5 Data may be read from the Readout Buffers only in extended non-privileged 64-bit block transfer mode.
- 3.8.6 The MASTER shall have a register that contains a unique identification number (ID PROM.) This register shall be read-only, accessible only in VME Mode using 64-bit block transfers. It contains 32 ASCII characters. See Appendices IV-V.
- 3.8.7 The VME backplane connector definition is given in Appendix II.
- 3.8.8 The definition of the address space used by the MASTER Module is given in Appendices IV-V.

### 3.9 Look-Up Tables

- 3.9.1 The raw QIE data has a format as given in Table 3.3. The data must be linearized (turned into a linear 16 bit number) by the MASTER Module in order to apply a threshold cut. It is also necessary to linearize the data if the data from several clock cycles are to be added together, as might be done by the event building process in the trigger farm.
- 3.9.2 The method used by the MASTER Module to linearize the QIE data shall be through the use of Look-Up Tables (LUTs.) With this method, the QIE data (capid + range + adc) along with the channel address form an address into a memory. Stored in that memory location is the equivalent 16-bit number for that value of QIE data for that particular channel and capacitor ID. The values are pre-determined using a calibration procedure, and loaded prior to taking data.
- 3.9.3 The output data bus of the LUT shall be 16 bits wide. The minimum size of the LUT for each MASTER input is specified as follows:

The number of possible codes per QIE channel is:

$$2^{*(8 \text{ ADC Bits} + 3 \text{ RANGE Bits} + 2 \text{ CAPID Bits})} = 8192 \text{ possible codes}$$

The size of the address space per MASTER Input Channel must accommodate 16 QIEs:

$$8192 * 16 \text{ QIEs/MINDER} = 128\text{K possible addresses}$$

- 3.9.4 There is no specified procedure for how to choose the values for the LUTs. The values are arbitrary from the perspective of the MASTER Module. The method for loading the LUTs is an operational issue. The MASTER Module shall be capable of operation for arbitrary values loaded into the LUT.
- 3.9.5 A method shall be provided to load the LUTs through VME data transfers from the ROP to the MASTER Module. See Appendices IV-V for a description of the MASTER memory map.
- 3.9.6 A method shall be provided to read the contents of the LUTs through VME data transfers from the MASTER Module to the ROP. See Appendices IV-V for a description of the MASTER memory map.
- 3.9.7 A method shall be provided to save the contents of the LUTs in a local flash memory on the MASTER Module. A method shall also be provided to reload the LUTs from a local flash memory. See Section 3.10 for a description of the flash memory and the Flash Register.

**3.10 Flash Memory & Flash Register**

- 3.10.1 The MASTER Module shall contain a local flash memory for each LUT. They will be used to store and recall the contents of the LUTs whenever the VME crate containing the MASTER Module is powered down, without the need for re-calibration.
- 3.10.2 A method shall be provided to save the contents of the LUTs in the flash memory through commands from the ROP. See Section 3.10.4.
- 3.10.3 A method shall be provided to load the contents of the LUTs from local flash memory on the MASTER Module when power is applied to the MASTER Module. This shall be an automatic procedure.
- 3.10.4 The MASTER Module shall contain a register called the Flash register, which controls the downloading (save LUT data to flash memory), uploading (recall LUT data from flash memory), and erasing (clear data from flash memory). The 32-bits of the Flash Register are defined in Table 3.8. Note that the MASTER must be in Flash Mode to perform flash memory operations, as described in Section 3.1. See Appendices IV-V for a description of the MASTER memory map.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	EDU			X	EDU			X	EDU			X	EDU			X	EDU			X	EDU			X	EDU			X	EDU		
	CH 7				CH 6				CH 5				CH 4				CH 3				CH 2				CH 1				CH 0		

U – Upload Flash Memory Data to LUT Memory  
 D – Download LUT Memory Data to Flash Memory  
 E – Erase Data from Flash Memory  
 X – Not Used

**Table 3.8 Definition of the Flash Register**

- 3.10.5 The general convention of downloading LUT memory data to Flash memory requires first that the Flash memory be erased. This is not an automatic operation. It assumed that this step is done as part of the protocol in the VME program control environment.

**3.11 Threshold Register**

- 3.11.1 The MASTER Module shall have a 16-bit register for storing the binary value of the threshold to be applied to the linearized QIE data.
- 3.11.2 The threshold value is used in Data Mode and Diagnostic data Mode. See Section 3.1.
- 3.11.3 Each input channel shall have a separate threshold register. The value loaded into a particular threshold register shall provide the threshold value for all of the MINDER channels associated with that input channel. See Appendices IV-V for the listing of the memory map.
- 3.11.4 The threshold shall function so that any linearized QIE data word that is greater than or equal to the value of the threshold shall be saved in the Readout Buffer.

**3.12 Status Register**

- 3.12.1 The Master Module shall have a 32-bit register for controlling the functionality of the module, and for reporting the status to the ROP.
- 3.12.2 The Status Register is defined as follows:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
FF[7:0]								FE[7:0]								X				D	X	I	X	MODE[2:0]							

- FF[7:0] – FIFO Full Flags for Input Channels 7 through 0
- FE[7:0] – FIFO Empty Flags for Input Channels 7 through 0
- X – Not Used
- D – Diagnostic Event in Progress (1 = in progress, 0 = done)
- I – Interrupt Request Enable on MINDER Error (0 = disable {default})
- MODE[2:0] – Operational Mode Bits (See Section 3.1)

**Table 3.9 Definition of the Status Register**

### 3.13 Error Reporting

3.13.1 The general technique for reporting data processing errors is to tag the data word associated with the occurrence of the error.

3.13.2 The MASTER Module shall detect the following types of errors associated with data processing:

a. Parity Errors

The MINDER Modules generate a parity bit on the 13 bits of raw QIE data, as given in Table 3.3, and as described in Section 3.2. The MASTER shall detect when any data word has a parity error, and shall assert the Parity Error Bit for that data word, as described in Section 3.13.3.

b. CAPID Errors

The generation of CAPIDs by the QIEs in the MINDER Crates is synchronized so that all the QIEs on a MINDER Module should have the same value of CAPID on any given clock cycle. When a data transfer sequence is initiated, the ordering of the data is as specified in Section 3.3. The ordering of the data is such that the value of the CAPIDs can be predicted after the first data word is read. The MASTER Module shall detect when any data word has an incorrect value of CAPID, based on the value of the CAPID on the first data word. When the MASTER detects a CAPID out of sequence, the CAPID Error Bit is asserted for that data word, as described in Section 3.13.3.

c. Word Count Errors

When a data transfer is initiated, a fixed number of data words are sent from the MINDER to the MASTER. The Header Bit marks the beginning of a data transmission, and the Trailer Bit marks the end. See Section 3.4. The MASTER shall detect when too many or too few words have been sent in a transmission sequence. The number of words sent depends on the type of data. See Section 3.3. While the number of words sent varies as a function of type of data, the number of words will always be a multiple of 16, since there are 16 QIE channels on each MINDER. It is sufficient for the MASTER to count QIE data words modulo 16, and detect an error when the word count is not 16 when the Trailer Bit is received. When this occurs, the MASTER shall assert the Word Count Error Bit on the last data word in the transmission sequence. See Section 3.13.3.

### 3.13 Error Reporting (Cont.)

3.13.2 The MASTER Module shall detect the following types of errors associated with data processing (continued):

d. Header Bit Error

The MINDER Modules set a Header Bit on the first word of a transmission sequence, and set a Trailer Bit on the last word. See Section 3.3. If a MINDER sends a second Header Bit before the Trailer Bit, then this creates uncertainty about the quality of the data sequence. The MASTER shall detect this error and report it. Since this is equivalent to a word count error, the MASTER shall report it in the same manner, by asserting the Word Count Error Bit on that data word. The MASTER shall then truncate the data processing for that transmission sequence, and begin a new one, using the second Header Bit as the start of the sequence.

e. Buffer Full Error

Because the Readout Buffers have a finite size, it is possible for a buffer to completely fill. If this happens, the MASTER shall continue reading data from the input FIFO (as described in Section 3.3 and Section 3.4), but no data will be written to the Readout Buffer. This causes data to be lost, but previous data is preserved. When the buffer fills completely, the MASTER shall assert the Word Count Error Bit on the last word written to the buffer. While this creates some ambiguity in the meaning of the Word Count Error Bit, the signature of the Buffer Full Error should be relatively easy to identify with proper online monitoring.

3.13.3 The errors defined in Section 3.13.2 shall be reported on the data word on which they occur. The format of the data words is different depending on the MASTER mode of operation, but the relative location of the error bits in the data word is the same, and the meaning of the bits is the same. See Section 3.4 and Section 3.5 for the data formats.

ERR[2] = Word Count Error Bit

ERR[1] = CAPID Error Bit

ERR[0] = Parity Error Bit

### 3.13 Error Reporting (Cont.)

3.13.4 There is a feature of the MINDER Modules in which they can prematurely abort a data transmission cycle. This can occur if the event being transferred from the MINDER to the MASTER is of a lower priority than one about to be acquired. (Data transmission and acquisition cycles do not overlap in this system.) In this case, the MINDER may abruptly stop the data transmission before all of the data has been sent. Without special provision, the MASTER would then generate a word count error. To prevent a word count error, the MINDER asserts the Error Bit on the data output at the same time that it asserts the Trailer Bit. When the MASTER reads the coincidence of these two bits, it process the associated data normally, and then ends the processing for that data transmission cycle without generating a word count error. See Section 3.2.

3.13.5 The KEEPER receives status bits from the modules in the MINDER crate. These signals indicate that there is a catastrophic error in the MINDER Crate, which could corrupt or otherwise compromise the data. The status bits are logically OR'd together on the KEEPER, and sent to the MASTER on a dedicated signal line on the control cable. When the MASTER receives this signal, it does the following:

- a. The MASTER writes a bit into a dedicated register, called the MINDER Error Register. See Appendices IV-V. The register can be queried by the ROP. The error bit stays set until it is cleared by the ROP.
- b. The MASTER can be enabled to generate a VME Interrupt Request when this signal is generated. Interrupt Request 5 is reserved for this function. The feature is enabled by setting a bit in the Status Register. See Section 3.12. This would inform the ROP immediately that there is an error in the MINDER Crate. The Interrupt Handler in the ROP then deals with the error, which may involve querying the modules in the MINDER Crate to find which module generated the error.

### 3.14 Reset and Clear Functions

- 3.14.1 A selected MASTER Module can be reset by the ROP. This is done by writing data to the Master Clear address on the MASTER Module. See Appendices IV-V.
- 3.14.2 The following operations are performed in response to a Master Clear command:
- a. The input FIFOs for all 8 input channels are reset.
  - b. All Channel Word Counters (16) and all Total Word Count Registers (2) are reset.
  - c. The Diagnostic Memory Address register is reset.
  - d. The Start Event Latches and Start Event Diagnostic Latches are initialized to write to Buffer 0.
- 3.14.3 The following are *NOT* reset in response to a MASTER Clear:
- a. The Status register is *NOT* cleared.
  - b. The Threshold Registers are *NOT* cleared.
  - c. The Flash Memories are *NOT* cleared.
  - d. The LUTs are *NOT* cleared.
  - e. The Diagnostic Memory is *NOT* cleared.
- 3.14.4 VME System Clear (SYSCLR) is used to reconfigure the programmable logic on the MASTER Module. Occasionally, the configuration of the logic can be corrupted. It is not always obvious when this has happened, but often it shows up as corrupted data or the inability of the ROP to communicate with the MASTER or MINDER Crate. When SYSCLR is issued by the ROP, it causes all of the programmable logic on the MASTER to be reconfigured from on-board PROMs. (This is done automatically at power-up.) Note that SYSCLR is broadcast to all modules residing in that VME crate, so that all MASTERS in the crate reconfigure at the same time.

### 3.14 Reset and Clear Functions (Cont.)

3.14.5 The following operations are performed in response to SYSCLR:

- a. All of the programmable logic is reconfigured from on-board PROM.
- b. All of the operations listed in Section 3.14.2 are executed.
- c. The Status register is cleared.
- d. The Threshold Registers are cleared.
- e. The Flash Register is cleared.
- f. The contents of the LUTs are reloaded from Flash Memory. If the LUTs were written to by the ROP but the contents not downloaded to Flash Memory, then the contents of the LUTs will be lost and replaced with that in the Flash Memory.

3.14.6 The following are *NOT* reset in response to SYSCLR:

- a. The Flash Memories are *NOT* cleared.
- c. The Diagnostic Memory is *NOT* cleared.

3.14.7 When the VME Crate is power-cycled (power turned off and then on,) reset operations are performed on the MASTER Module. These include:

- a. All of the operations listed in Section 3.14.5 are executed.
- b. The contents of the Diagnostic memory are lost.

3.14.8 The following are *NOT* reset in response to power-cycling: The Flash Memory is *NOT* cleared.

### 3.15 Control of MINDER Crate

- 3.15.1 The MASTER shall provide slow control functions to the MINDER Crate.
- 3.15.2 The MINDER Crate Controller is called the KEEPER. The MASTER communicates with the KEEPER.
- 3.15.3 One MASTER may communicate with one and only one KEEPER. The KEEPER shall communicate with one and only one MASTER.
- 3.15.4 The connector for the data transmission between the KEEPER and the MASTER is located on the J3 connector of the MASTER Module. The J3 shall be a straight feed-through of signals.
- 3.15.5 The data transmission between the KEEPER and the MASTER is bi-directional.
- 3.15.6 The logic family used for data transmission is LVDS.
- 3.15.7 The addressing between the MASTER and the KEEPER shall be memory-mapped into the VME address space of the MASTER Module.
- 3.15.8 The signal definition and pin-out for the data transmission between the KEEPER and the MASTER Module is defined in Appendix III.
- 3.15.9 A means shall be provided for acquiring data through a process initiated by the ROP in the MASTER Crate. Called the VME Trigger, this will be used to acquire pedestal and calibration data, initiate diagnostic events, and perform other diagnostics. See Appendices IV-V for the memory map.

### 3.16 Clock for the MASTER

- 3.16.1 The MASTER shall use SYSCLK from the VME backplane.
- 3.16.2 The frequency of the clock shall be 26.5 MHz (half of the Main Injector RF clock frequency.)
- 3.16.3 The MASTER shall not have an on-board oscillator.

#### 4. Bibliography

- [1] G. Drake, J. Dawson, C. Nelson, "Overview of the Front End Electronics for the MINOS Near Detector," Version 1.35, NUMI Internal Note NUMI-L-628, Nov. 15, 1999.
- [2] The CDF II Detector, Technical Design Report, November, 1996.
- [3] J. Dawson, G. Drake, C. Nelson, S. Madani, T. Nicholls, G. Pearce, "Conceptual Design of the VME Interface for the MINOS Near Detector," Version 2.3, NUMI Internal Note NUMI-L-627, May 3, 2000.
- [4] R.J.Yarema et. al., A Fast, Wide Range Charge Integrator and Encoder ASIC for Photomultiplier Tubes, IEEE Trans. on Nuclear Science, Vol. 4, August, 1993, pp. 750-752.
- [5] R.J.Yarema, et. al., "A High Speed, Wide Dynamic Range Digitizer Circuit for Photomultiplier Tubes," Presented at the 6th Pisa Meeting on Advanced Detectors, May 22-28, 1994, La Biodola, Isola d'Elba, Italy.
- [6] VME64 Specifications, IEEE Specification IEEE 1014-1987.
- [7] VME64 Specifications, ANSI/VITA 1-1994
- [8] VME64X Specifications, ANSI/VITA 1.1-1997
- [9] Wade D. Peterson, "VMEbus Handbook Specifications," 4th Edition, VITA, 1997.

## 5. Appendices

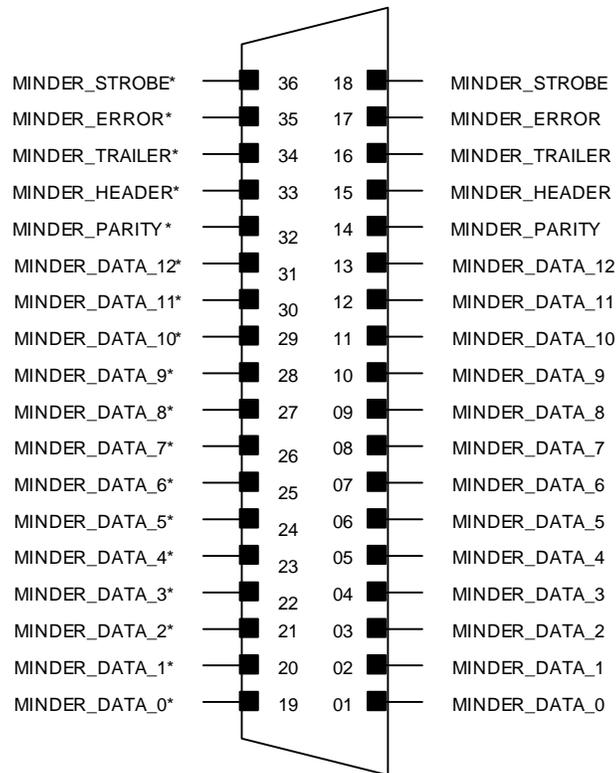
### 5.1 Appendix I – Definition of Data Input Connector

5.1.1 Manufacturer: 3M

5.1.2 Type: Mini D Ribbon Connector  
0.050" Boardmount R.A. Receptacle, 36 pos.

5.1.3 Part Number: 10236-55G3VC

5.1.4 Pin Out:



**Figure 5.1 View Into Front of PCB Mount Data Connector**

### 5. Appendices (Cont.)

#### 5.2 Appendix II – Definition of VME Backplane Connector

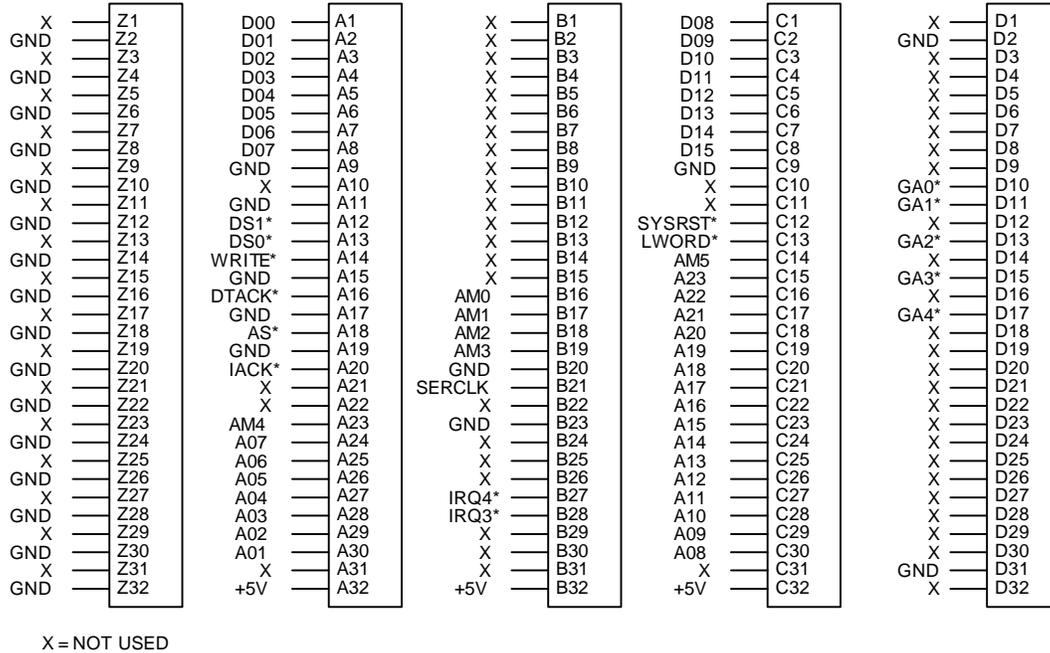


Figure 5.2 VME J1 Connector - View Into Front of Crate

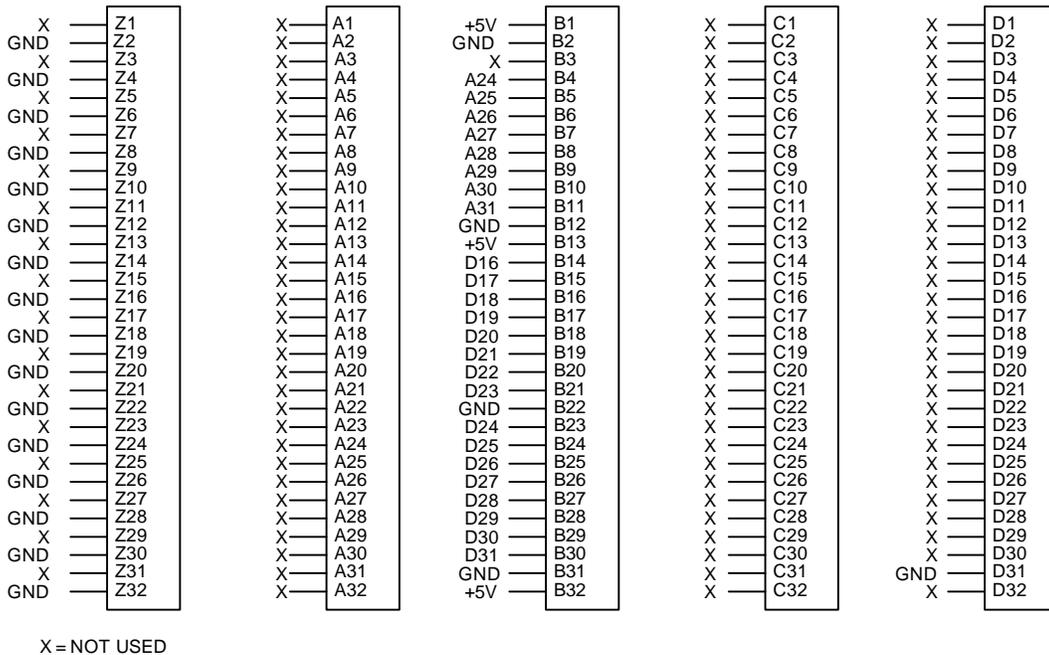
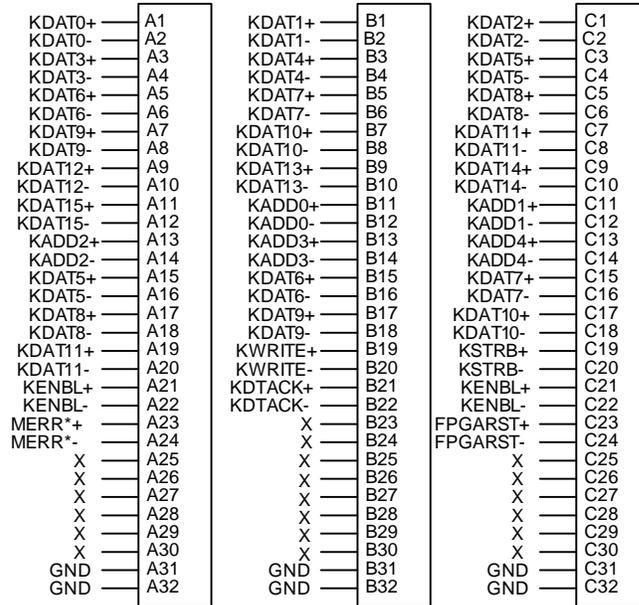


Figure 5.3 VME J2 Connector - View Into Front of Crate

5. Appendices (Cont.)

5.3 Appendix III – Definition of KEEPER Interface



X = NOT USED

Figure 5.4 VME J3 Connector - View Into Front of Crate

5. Appendices (Cont.)

5.4 Appendix IV – Definition of VME Address Space - Version 1 MASTER

MINOS MASTER Card VME Function Addresses

9/25/01

VME base address (A31-A27) is configured by the Geographical Address pins (GA4-GA0).  
The only Address Modifiers that the Card will respond to are:

- 1. Extended non-privileged 64-bit block transfer (64-bit, 32 address block transfers) AM=08
- 2. Extended non-privileged data access (32-bit, 32 address single transfers) AM=09
- 3. Extended non-privileged block transfer (32-bit, 32 address block transfers) AM=0B

Address Modifier	Hex Address (h) Offset (A26-A2)	Function
-----		
Data Format of Dual Port BUFFER output data		
-----		
D26-D0 = Timestamp TS[26..0]		
D28-D27 = Reserved X[1..0]		
D31-D29 = Data Type DT[2..0]		
D47-D32 = ADC Value ADC[15..0]		
D52-D48 = MINDER Channel Number CH[4..0]		
D55-D53 = MASTER Input Channel Number ICH[2..0]		
D60-D56 = Geographical Address GA[4..0]		
D63-D61 = Error Codes ERR[2..0]		
ERR0 = Input Parity Error 1=Error		
ERR1 = Capacitor ID Error 1=Error		
ERR2 = Trailer Ch. Num. Error, or 1=Error		
Two Headers before Trailer, or		
>= 8192 Words written to buffer		
08	h0000000	READ only – Dual Port BUFFER 0 (All channels with data) (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D63-D0 = Data
08	h0080000	READ only – Dual Port BUFFER 1 (All channels with data) (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D63-D0 = Data
08	h1000000- h100FFF8	READ only – Channel 0, Dual Port BUFFER 0 (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D63-D0 = Data
08	h1010000- h101FFF8	READ only – Channel 0, Dual Port BUFFER 1 (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D63-D0 = Data

## 5. Appendices (Cont.)

### 5.4 Appendix IV – Definition of VME Address Space - Version 1 (Cont.)

08	h1020000- h102FFF8	READ only – Channel 1, Dual Port BUFFER 0 (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D63-D0 = Data
08	h1030000- h103FFF8	READ only – Channel 1, Dual Port BUFFER 1 (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D63-D0 = Data
08	h1040000- h104FFF8	READ only – Channel 2, Dual Port BUFFER 0 (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D63-D0 = Data
08	h1050000- h105FFF8	READ only – Channel 2, Dual Port BUFFER 1 (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D63-D0 = Data
08	h1060000- h106FFF8	READ only – Channel 3, Dual Port BUFFER 0 (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D63-D0 = Data
08	h1070000- h107FFF8	READ only – Channel 3, Dual Port BUFFER 1 (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D63-D0 = Data
08	h1080000- h108FFF8	READ only – Channel 4, Dual Port BUFFER 0 (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D63-D0 = Data
08	h1090000- h109FFF8	READ only – Channel 4, Dual Port BUFFER 1 (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D63-D0 = Data
08	h10A0000- h10AFFF8	READ only – Channel 5, Dual Port BUFFER 0 (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D63-D0 = Data
08	h10B0000- h10BFFF8	READ only – Channel 5, Dual Port BUFFER 1 (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D63-D0 = Data

## 5. Appendices (Cont.)

### 5.4 Appendix IV – Definition of VME Address Space - Version 1 (Cont.)

08	h10C0000- h10CFFF8	READ only – Channel 6, Dual Port BUFFER 0 (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D63-D0 = Data
08	h10D0000- h10DFFF8	READ only – Channel 6, Dual Port BUFFER 1 (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D63-D0 = Data
08	h10E0000- h10EFFF8	READ only – Channel 7, Dual Port BUFFER 0 (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D63-D0 = Data
08	h10F0000- h10FFFF8	READ only – Channel 7, Dual Port BUFFER 1 (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D63-D0 = Data
08	h2000000- h21FFFF8	WRITE/READ – Channel 0, 1, 2, & 3 Look-Up-Table Memory (Must be in VME Mode) D15-D0 = Channel 0 data D31-D16 = Channel 1 data D47-D32 = Channel 2 data D63-D48 = Channel 3 data
08	h2200000- h23FFFF8	WRITE/READ – Channel 4, 5, 6, & 7 Look-Up-Table Memory (Must be in VME Mode) D15-D0 = Channel 4 data D31-D16 = Channel 5 data D47-D32 = Channel 6 data D63-D48 = Channel 7 data
09	h0000000	WRITE/READ – Status Register (Bits D31-D16 are READ only) See data pattern below

5. Appendices (Cont.)

5.4 Appendix IV – Definition of VME Address Space - Version 1 (Cont.)

09                    h0000004                    WRITE/READ – Flash Register  
 (Must be in Flash Mode) See data pattern below

Bit	Status Register	Flash Register
-----	-----	-----
D0	* Mode 0	UPLD Ch 0
D1	* Mode 1	DNLD Ch 0
D2	* Mode 2	ERAS Ch 0
D3		
D4		UPLD Ch 1
D5		DNLD Ch 1
D6		ERAS Ch 1
D7	Diagnostic Event in progress	
D8		UPLD Ch 2
D9		DNLD Ch 2
D10		ERAS Ch 2
D11		
D12		UPLD Ch 3
D13		DNLD Ch 3
D14		ERAS Ch 3
D15		
D16	FIFO 0 MT (RO)	UPLD Ch 4
D17	FIFO 1 MT (RO)	DNLD Ch 4
D18	FIFO 2 MT (RO)	ERAS Ch 4
D19	FIFO 3 MT (RO)	
D20	FIFO 4 MT (RO)	UPLD Ch 5
D21	FIFO 5 MT (RO)	DNLD Ch 5
D22	FIFO 6 MT (RO)	ERAS Ch 5
D23	FIFO 7 MT (RO)	
D24	FIFO 0 FL (RO)	UPLD Ch 6
D25	FIFO 1 FL (RO)	DNLD Ch 6
D26	FIFO 2 FL (RO)	ERAS Ch 6
D27	FIFO 3 FL (RO)	
D28	FIFO 4 FL (RO)	UPLD Ch 7
D29	FIFO 5 FL (RO)	DNLD Ch 7
D30	FIFO 6 FL (RO)	ERAS Ch 7
D31	FIFO 7 FL (RO)	

Note: Diagnostic Event bit = 1 during sending of diagnostic data but = 0  
 when Diagnostic Event is done

(RO) = READ only bits

MT = Empty

FL = Full

UPLD = Upload Flash Memory data to Look-Up-Table Memory

DNLD = Download Look-Up-Table Memory data to Flash Memory

ERAS = Erase Flash Memory

(Continued Next Page)

5. Appendices (Cont.)

5.4 Appendix IV – Definition of VME Address Space - Version 1 (Cont.)

*Mode 2	Mode 1	Mode 0	
-----	-----	-----	
0	0	0	Standby Mode
0	0	1	Data Mode
0	1	0	Calibration Mode
0	1	1	Flash Mode
1	0	0	VME Mode
1	0	1	Diagnostic Data Mode
1	1	0	Diagnostic Calibration Mode
1	1	1	

09	h0000008	WRITE only – Master Clear D31-D0 = No data needed
09	h0004000	READ only – Channel 0, BUFFER 0 Word Counter (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D12-D0 = Channel 0 data D15-D13 = 0 D31-D16 = Undefined
09	h0004004	READ only – Channel 1, BUFFER 0 Word Counter (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D12-D0 = Channel 1 data D15-D13 = 0 D31-D16 = Undefined
09	h0004008	READ only – Channel 2, BUFFER 0 Word Counter (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D12-D0 = Channel 2 data D15-D13 = 0 D31-D16 = Undefined
09	h000400C	READ only – Channel 3, BUFFER 0 Word Counter (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D12-D0 = Channel 3 data D15-D13 = 0 D31-D16 = Undefined
09	h0004010	READ only – Channel 4, BUFFER 0 Word Counter (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D12-D0 = Channel 4 data D15-D13 = 0 D31-D16 = Undefined

## 5. Appendices (Cont.)

### 5.4 Appendix IV – Definition of VME Address Space - Version 1 (Cont.)

09	h0004014	<p>READ only – Channel 5, BUFFER 0 Word Counter                      (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode)                      D12-D0 = Channel 5 data                      D15-D13 = 0                      D31-D16 = Undefined</p>
09	h0004018	<p>READ only – Channel 6, BUFFER 0 Word Counter                      (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode)                      D12-D0 = Channel 6 data                      D15-D13 = 0                      D31-D16 = Undefined</p>
09	h000401C	<p>READ only – Channel 7, BUFFER 0 Word Counter                      (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode)                      D12-D0 = Channel 7 data                      D15-D13 = 0                      D31-D16 = Undefined</p>
09	h0004020	<p>READ only – Channel 0, BUFFER 1 Word Counter                      (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode)                      D12-D0 = Channel 0 data                      D15-D13 = 0                      D31-D16 = Undefined</p>
09	h0004024	<p>READ only – Channel 1, BUFFER 1 Word Counter                      (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode)                      D12-D0 = Channel 1 data                      D15-D13 = 0                      D31-D16 = Undefined</p>
09	h0004028	<p>READ only – Channel 2, BUFFER 1 Word Counter                      (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode)                      D12-D0 = Channel 2 data                      D15-D13 = 0                      D31-D16 = Undefined</p>
09	h000402C	<p>READ only – Channel 3, BUFFER 1 Word Counter                      (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode)                      D12-D0 = Channel 3 data                      D15-D13 = 0                      D31-D16 = Undefined</p>

## 5. Appendices (Cont.)

### 5.4 Appendix IV – Definition of VME Address Space - Version 1 (Cont.)

09	h0004030	<p>READ only – Channel 4, BUFFER 1 Word Counter                      (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode)                      D12-D0 = Channel 4 data                      D15-D13 = 0                      D31-D16 = Undefined</p>
09	h0004034	<p>READ only – Channel 5, BUFFER 1 Word Counter                      (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode)                      D12-D0 = Channel 5 data                      D15-D13 = 0                      D31-D16 = Undefined</p>
09	h0004038	<p>READ only – Channel 6, BUFFER 1 Word Counter                      (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode)                      D12-D0 = Channel 6 data                      D15-D13 = 0                      D31-D16 = Undefined</p>
09	h000403C	<p>READ only – Channel 7, BUFFER 1 Word Counter                      (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode)                      D12-D0 = Channel 7 data                      D15-D13 = 0                      D31-D16 = Undefined</p>
09	h0004040	<p>READ only – BUFFER 0 Total Word Counter                      (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode)                      D15-D0 = BUFFER 0 data                      D31-D16 = Undefined</p>
09	h0004044	<p>READ only – BUFFER 1 Total Word Counter                      (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode)                      D15-D0 = BUFFER 1 data                      D31-D16 = Undefined</p>
09	h0008000	<p>WRITE/READ – Channel 0 &amp; 1 Threshold Register                      (Must be in VME Mode)                      D15-D0 = Channel 0 data                      D31-D16 = Channel 1 data</p>
09	h0008004	<p>WRITE/READ – Channel 2 &amp; 3 Threshold Register                      (Must be in VME Mode)                      D15-D0 = Channel 2 data                      D31-D16 = Channel 3 data</p>

## 5. Appendices (Cont.)

### 5.4 Appendix IV – Definition of VME Address Space - Version 1 (Cont.)

09	h0008008	<p>WRITE/READ – Channel 4 &amp; 5 Threshold Register                  (Must be in VME Mode)                  D15-D0 = Channel 4 data                  D31-D16 = Channel 5 data</p>
09	h000800C	<p>WRITE/READ – Channel 6 &amp; 7 Threshold Register                  (Must be in VME Mode)                  D15-D0 = Channel 6 data                  D31-D16 = Channel 7 data</p>
09	h000C000	<p>WRITE only – Start Strobing Diagnostic Data to BUFFER 0                  (Must be in Diagnostic Data or Diagnostic Calibrate Mode)                  D26-D0 = Timestamp                  D28-D27 = 0                  D31-D29 = Data Type</p>
09	h000C004	<p>WRITE only – Start Strobing Diagnostic Data to BUFFER 1                  (Must be in Diagnostic Data or Diagnostic Calibrate Mode)                  D26-D0 = Timestamp                  D28-D27 = 0                  D31-D29 = Data Type</p>
09	h000C008	<p>WRITE only – Load Diagnostic Memory Starting Address                  (Must be in VME Mode)                  D17-D0 = Starting address data                  D31-D18 = No data needed</p>
09	h000C00C	<p>WRITE only – Clear Diagnostic Memory Address Register                  D31-D0 = No data needed</p>
09	h0014000- h0017FFC	<p>WRITE/READ – MINDER Crate                  D15-D0 = Data                  D31-D16 = Undefined                  Note: Writing to address h0014230 (VME Strobe to Buffer 0) or to address h0014234 (VME Strobe to Buffer 1) on the TRIGGER-KEEPER Card will set the buffer on the MASTER Card also.</p>
0B	h0000000- h00FFFFC	<p>WRITE/READ – Diagnostic Memory                  (Must be in VME Mode)                  D7-D0 = Diagnostic data - ADC bits                  D10-D8 = Diagnostic data - Range bits                  D12-D11 = Diagnostic data - CAPID bits                  D13 = Diagnostic data - Parity bit                  D14 = Diagnostic data - Header bit (Should always = 0)                  D15 = Diagnostic data - Trailer bit (Always = 0, except for the last data word for that event, then = 1)                  D31-D16 = Undefined</p>

## 5. Appendices (Cont.)

### 5.4 Appendix IV – Definition of VME Address Space - Version 1 (Cont.)

0B	h1000000- h100007C	READ only - ID PROM D31-D24 = ASCII data for all ID PROM addresses D23-D0 = Undefined
----	-----------------------	---

5. Appendices (Cont.)

5.5 Appendix V – Definition of VME Address Space - Version 2

MINOS MASTER Card VME Function Addresses  
(For Revision A Cards)

4/3/02

VME base address (A31-A27) is configured by the Geographical Address pins (GA4-GA0).  
The only Address Modifiers that the Card will respond to are:

1. Extended non-privileged 64-bit block transfer (64-bit data, 32-bit address block transfers) AM=08
2. Extended non-privileged data access (32-bit data, 32-bit address single transfers) AM=09

Address Modifier	Hex Address (h) Offset (A26-A2)	Function
-----		
Data Format of Dual Port BUFFER output data		
-----		
D26-D0 = Timestamp TS[26..0] D28-D27 = Reserved X[1..0] D31-D29 = Data Type DT[2..0] D47-D32 = ADC Value ADC[15..0] D52-D48 = MINDER Channel Number CH[4..0] D55-D53 = MASTER Input Channel Number ICH[2..0] D60-D56 = Geographical Address GA[4..0] D63-D61 = Error Codes ERR[2..0] ERR0 = Input Parity Error 1=Error ERR1 = Capacitor ID Error 1=Error ERR2 = Trailer Ch. Num. Error, or 1=Error Two Headers before Trailer, or >= 16384 Words written to a channel's buffer		
08	h0000000	READ only – Dual Port BUFFER 0 (All channels with data) (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D63-D0 = Data
08	h0100000	READ only – Dual Port BUFFER 1 (All channels with data) (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D63-D0 = Data
08	h1000000- h101FFF8	READ only – Channel 0, Dual Port BUFFER 0 (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D63-D0 = Data
08	h1020000- h103FFF8	READ only – Channel 0, Dual Port BUFFER 1 (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D63-D0 = Data

## 5. Appendices (Cont.)

### 5.5 Appendix V – Definition of VME Address Space - Version 2 (Cont.)

08	h1040000- h105FFF8	READ only – Channel 1, Dual Port BUFFER 0 (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D63-D0 = Data
08	h1060000- h107FFF8	READ only – Channel 1, Dual Port BUFFER 1 (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D63-D0 = Data
08	h1080000- h109FFF8	READ only – Channel 2, Dual Port BUFFER 0 (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D63-D0 = Data
08	h10A0000- h10BFFF8	READ only – Channel 2, Dual Port BUFFER 1 (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D63-D0 = Data
08	h10C0000- h10DFFF8	READ only – Channel 3, Dual Port BUFFER 0 (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D63-D0 = Data
08	h10E0000- h10FFFF8	READ only – Channel 3, Dual Port BUFFER 1 (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D63-D0 = Data
08	h1100000- h111FFF8	READ only – Channel 4, Dual Port BUFFER 0 (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D63-D0 = Data
08	h1120000- h113FFF8	READ only – Channel 4, Dual Port BUFFER 1 (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D63-D0 = Data
08	h1140000- h115FFF8	READ only – Channel 5, Dual Port BUFFER 0 (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D63-D0 = Data
08	h1160000- h117FFF8	READ only – Channel 5, Dual Port BUFFER 1 (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D63-D0 = Data

## 5. Appendices (Cont.)

### 5.5 Appendix V – Definition of VME Address Space - Version 2 (Cont.)

08	h1180000- h119FFF8	<p>READ only – Channel 6, Dual Port BUFFER 0 (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D63-D0 = Data</p>
08	h11A0000- h11BFFF8	<p>READ only – Channel 6, Dual Port BUFFER 1 (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D63-D0 = Data</p>
08	h11C0000- h11DFFF8	<p>READ only – Channel 7, Dual Port BUFFER 0 (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D63-D0 = Data</p>
08	h11E0000- h11FFFF8	<p>READ only – Channel 7, Dual Port BUFFER 1 (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D63-D0 = Data</p>
08	h2000000- h20FFFF8	<p>WRITE/READ – Channel 0, 1, 2, &amp; 3 Look-Up-Table Memory (Must be in VME Mode) D15-D0 = Channel 0 data D31-D16 = Channel 1 data D47-D32 = Channel 2 data D63-D48 = Channel 3 data</p>
08	h2100000- h21FFFF8	<p>WRITE/READ – Channel 4, 5, 6, &amp; 7 Look-Up-Table Memory (Must be in VME Mode) D15-D0 = Channel 4 data D31-D16 = Channel 5 data D47-D32 = Channel 6 data D63-D48 = Channel 7 data</p>
08	h2200000- h23FFFF8	<p>WRITE/READ – Diagnostic Memory (Must be in VME Mode) D7-D0 = Diagnostic data - ADC bits D10-D8 = Diagnostic data - Range bits D12-D11 = Diagnostic data - CAPID bits D13 = Diagnostic data - Parity bit D14 = Diagnostic data - Header bit (Should always = 0) D15 = Diagnostic data - Trailer bit (Always = 0, except for the last data word for that event, then = 1) D16 = Diagnostic data – Priority error bit D63-D17 = Undefined</p>

5. Appendices (Cont.)

5.5 Appendix V – Definition of VME Address Space - Version 2 (Cont.)

08	h2400000- h24000F8	READ only - ID PROM (Can read in any Mode) D31-D24 = ASCII data for all ID PROM addresses D63-D32 = Undefined D23-D0 = Undefined
09	h0000000	WRITE/READ – Status Register (Bits D31-D16 are READ only) See data pattern below
09	h0000004	WRITE/READ – Flash Register (Must be in Flash Mode) See data pattern below

Bit	Status Register	Flash Register
----	-----	-----
D0	* Mode 0	UPLD Ch 0
D1	* Mode 1	DNLD Ch 0
D2	* Mode 2	ERAS Ch 0
D3		
D4	Interrupt Mask bit Interrupt Enabled = 1	UPLD Ch 1
D5		DNLD Ch 1
D6		ERAS Ch 1
D7	Diagnostic Event in progress	
D8		UPLD Ch 2
D9		DNLD Ch 2
D10		ERAS Ch 2
D11		
D12		UPLD Ch 3
D13		DNLD Ch 3
D14		ERAS Ch 3
D15		
D16	FIFO 0 MT (RO)	UPLD Ch 4
D17	FIFO 1 MT (RO)	DNLD Ch 4
D18	FIFO 2 MT (RO)	ERAS Ch 4
D19	FIFO 3 MT (RO)	
D20	FIFO 4 MT (RO)	UPLD Ch 5
D21	FIFO 5 MT (RO)	DNLD Ch 5
D22	FIFO 6 MT (RO)	ERAS Ch 5
D23	FIFO 7 MT (RO)	
D24	FIFO 0 FL (RO)	UPLD Ch 6
D25	FIFO 1 FL (RO)	DNLD Ch 6
D26	FIFO 2 FL (RO)	ERAS Ch 6
D27	FIFO 3 FL (RO)	
D28	FIFO 4 FL (RO)	UPLD Ch 7
D29	FIFO 5 FL (RO)	DNLD Ch 7
D30	FIFO 6 FL (RO)	ERAS Ch 7
D31	FIFO 7 FL (RO)	

(Continued next page)

5. Appendices (Cont.)

5.5 Appendix V – Definition of VME Address Space - Version 2 (Cont.)

Note: Diagnostic Event bit = 1 during sending of diagnostic data but = 0 when Diagnostic Event is done

(RO) = READ only bits

MT = Empty

FL = Full

UPLD = Upload Flash Memory data to Look-Up-Table Memory

DNLD = Download Look-Up-Table Memory data to Flash Memory

ERAS = Erase Flash Memory

*Mode 2	Mode 1	Mode 0	
-----	-----	-----	
0	0	0	Standby Mode
0	0	1	Data Mode
0	1	0	Calibration Mode
0	1	1	Flash Mode
1	0	0	VME Mode
1	0	1	Diagnostic Data Mode
1	1	0	Diagnostic Calibration Mode
1	1	1	

09	h0000008	WRITE only – Master Clear D31-D0 = No data needed
09	h000000C	WRITE/READ – Minder Crate Error Register D0 = Error Bit D31-D1 = Undefined
09	h0004000	READ only – Channel 0, BUFFER 0 Word Counter (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D13-D0 = Channel 0 data D15-D14 = 0 D31-D16 = Undefined
09	h0004004	READ only – Channel 1, BUFFER 0 Word Counter (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D13-D0 = Channel 1 data D15-D14 = 0 D31-D16 = Undefined
09	h0004008	READ only – Channel 2, BUFFER 0 Word Counter (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D13-D0 = Channel 2 data D15-D14 = 0 D31-D16 = Undefined

## 5. Appendices (Cont.)

### 5.5 Appendix V – Definition of VME Address Space - Version 2 (Cont.)

09	h000400C	<p>READ only – Channel 3, BUFFER 0 Word Counter                      (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode)                      D13-D0 = Channel 3 data                      D15-D14 = 0                      D31-D16 = Undefined</p>
09	h0004010	<p>READ only – Channel 4, BUFFER 0 Word Counter                      (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode)                      D13-D0 = Channel 4 data                      D15-D14 = 0                      D31-D16 = Undefined</p>
09	h0004014	<p>READ only – Channel 5, BUFFER 0 Word Counter                      (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode)                      D13-D0 = Channel 5 data                      D15-D14 = 0                      D31-D16 = Undefined</p>
09	h0004018	<p>READ only – Channel 6, BUFFER 0 Word Counter                      (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode)                      D13-D0 = Channel 6 data                      D15-D14 = 0                      D31-D16 = Undefined</p>
09	h000401C	<p>READ only – Channel 7, BUFFER 0 Word Counter                      (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode)                      D13-D0 = Channel 7 data                      D15-D14 = 0                      D31-D16 = Undefined</p>
09	h0004020	<p>READ only – Channel 0, BUFFER 1 Word Counter                      (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode)                      D13-D0 = Channel 0 data                      D15-D14 = 0                      D31-D16 = Undefined</p>
09	h0004024	<p>READ only – Channel 1, BUFFER 1 Word Counter                      (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode)                      D13-D0 = Channel 1 data                      D15-D14 = 0                      D31-D16 = Undefined</p>

## 5. Appendices (Cont.)

### 5.5 Appendix V – Definition of VME Address Space - Version 2 (Cont.)

09	h0004028	READ only – Channel 2, BUFFER 1 Word Counter (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D13-D0 = Channel 2 data D15-D14 = 0 D31-D16 = Undefined
09	h000402C	READ only – Channel 3, BUFFER 1 Word Counter (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D13-D0 = Channel 3 data D15-D14 = 0 D31-D16 = Undefined
09	h0004030	READ only – Channel 4, BUFFER 1 Word Counter (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D13-D0 = Channel 4 data D15-D14 = 0 D31-D16 = Undefined
09	h0004034	READ only – Channel 5, BUFFER 1 Word Counter (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D13-D0 = Channel 5 data D15-D14 = 0 D31-D16 = Undefined
09	h0004038	READ only – Channel 6, BUFFER 1 Word Counter (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D13-D0 = Channel 6 data D15-D14 = 0 D31-D16 = Undefined
09	h000403C	READ only – Channel 7, BUFFER 1 Word Counter (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D13-D0 = Channel 7 data D15-D14 = 0 D31-D16 = Undefined
09	h0004040	READ only – BUFFER 0 Total Word Counter (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D16-D0 = BUFFER 0 data D31-D17 = Undefined

## 5. Appendices (Cont.)

### 5.5 Appendix V – Definition of VME Address Space - Version 2 (Cont.)

09	h0004044	READ only – BUFFER 1 Total Word Counter (Must be in Data, Calibrate, Diagnostic Data, or Diagnostic Calibrate Mode) D16-D0 = BUFFER 1 data D31-D17 = Undefined
09	h0008000	WRITE/READ – Channel 0 & 1 Threshold Register (Must be in VME Mode) D15-D0 = Channel 0 data D31-D16 = Channel 1 data
09	h0008004	WRITE/READ – Channel 2 & 3 Threshold Register (Must be in VME Mode) D15-D0 = Channel 2 data D31-D16 = Channel 3 data
09	h0008008	WRITE/READ – Channel 4 & 5 Threshold Register (Must be in VME Mode) D15-D0 = Channel 4 data D31-D16 = Channel 5 data
09	h000800C	WRITE/READ – Channel 6 & 7 Threshold Register (Must be in VME Mode) D15-D0 = Channel 6 data D31-D16 = Channel 7 data
09	h000C000	WRITE only – Start Strobing Diagnostic Data to BUFFER 0 (Must be in Diagnostic Data or Diagnostic Calibrate Mode) D26-D0 = Timestamp D28-D27 = 0 D31-D29 = Data Type
09	h000C004	WRITE only – Start Strobing Diagnostic Data to BUFFER 1 (Must be in Diagnostic Data or Diagnostic Calibrate Mode) D26-D0 = Timestamp D28-D27 = 0 D31-D29 = Data Type
09	h000C008	WRITE only – Load Diagnostic Memory Starting Address (Must be in VME Mode) D17-D0 = Starting address data D31-D18 = No data needed
09	h000C00C	WRITE only – Clear Diagnostic Memory Address Register D31-D0 = No data needed

## 5. Appendices (Cont.)

### 5.5 Appendix V – Definition of VME Address Space - Version 2 (Cont.)

09	h0014000- h0017FFC	WRITE/READ – MINDER Crate D15-D0 = Data D31-D16 = Undefined
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Note: Writing to address h0014230 (VME Strobe to Buffer 0) or to address h0014234 (VME Strobe to Buffer 1) on the TRIGGER-KEEPER Card will set the buffer on the MASTER Card also.

## 5. Appendices (Cont.)

### 5.6 Appendix VI – Generation of a VME Trigger

A VME Trigger is used to generate an event by the ROP. Typically, it is used to obtain pedestals or data from DC Current Calibrations. The generation of a VME Trigger is technically not part of the MASTER Module functionality or specification. The trigger actually occurs in response to writing to a register on the KEEPER. However, the MASTER "spies" on the transactions sent to the KEEPER, performs certain functions in the case when a VME Trigger is generated. In particular, the selection of the Readout Buffer is made in Calibration Mode by the VME address that is written to by the ROP. Two addresses are used, one Readout Buffer 0 and one for Readout Buffer 1. The data processing in the MINDER Crate does not use any information about the Readout Buffer. The two signals created by writing to these register locations are OR'ed together on the KEEPER, creating one VME Trigger signal, which is sent to the front end boards. Note that the data that is written to the register locations is irrelevant.

For the KEEPER location in slot 1, the register locations to create a VME Trigger are:

<b>Hex Address (h) Offset (A26-A2)</b>	<b>Selected Readout Buffer</b>
H0014230	Buffer 0
H0014234	Buffer 1

**Table 5.1 VME Addresses for Generating VME Triggers**