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FTBF TDC System Data Format Description

There are two eight port RJ-45 jacks on the controller forming two rows and eight columns. The TDC port numbers are mapped onto these jacks as shown:

1	3	5	7	9	11	13	15
2	4	6	8	10	12	14	16

The spill data contains a controller header followed by up to 16 TDC headers followed by TDC event data. Each TDC event block contains its own header, followed by data consisting of a six bit channel number appended to 10 bits of time data. Multiple hits on a channel within a gate will repeat the channel number. For events with no hits, the TDCs will send just the event header. Word counts include themselves, any associated header words, and all data words. The real time clock (RTC) data uses one byte to represent two BCD digits. As an aid to readout, the controller spill word count is accessible in a separate register so that a block move of a specified size can be set up in the host before a readout request is sent.

The controller spill TDC status word contains one bit per TDC. A zero indicates no errors for that TDC occurred during the spill, a one indicates one or more errors did occur. The individual TDC event status words can be used to further localize the point at which an error occurred. A series of diagnostic registers in the TDCs readable through the control path are provided as a debugging tool. The link status word will flag any errors that occurred while sending TDC data to the controller. The controller has its own set of diagnostic registers to help localize any errors of this type. The TDC spill status word indicates if any errors occurred during the spill for a particular TDC, and contains more bits to better indentify the error source.

The order of the data in the Ethernet data is: controller header followed by up to 16 TDC spill headers followed by event data. TDC data is channel ordered from lowest to highest port connection within an event and this structure is repeated for all subsequent events.

Controller Header words:

1	15..0	
	Total Spill word count bits 31..16	
2	15..0	
	Total Spill word count bits 15..0	
3	15..0	
	Spill Counter	
4	15..8	7..0
	RTC Year	RTC Month
5	15..8	7..0
	RTC Days	RTC Hours
6	15..8	7..0
	RTC Minutes	RTC Seconds
7	15..0	
	Spill Trigger Count bits 31..16	
8	15..0	
	Spill Trigger Count bits 15..0	
9	15..0	
	Spill Status Bits for TDCs	
10	15..0	
	Spill Link Status Bits	

TDC Spill Header words:

1	15..0	
	Total Spill Word Count for this TDC bits 31..16	
2	15..0	
	Total Spill Word Count for this TDC bits 15..0	
3	15..4	3..0
	Not Assigned	TDC #
4	15..0	
	Spill Trigger Count bits 31..16	
5	15..0	
	Spill Trigger Count bits 15..0	
6	15..8	7..0
	Not Assigned	Spill Status

TDC Event Header:

1	15..8	7..0
	Not Assigned	Event Word Count
2	15..4	3..0
	Not Assigned	TDC #
3	15..8	7..0
	Not Assigned	Event Status
4	15..0	
	Trigger Counter bits 31..16	
5	15..0	
	Trigger Counter bits 15..0	
6	15..4	3..0
	Not Assigned	Trigger Type
7	15..12	11..0
	Not Assigned	Event Time Stamp sent by the controller
8	31..16	
	TDC Event Time Stamp Upper Bits	
9	15..0	
	TDC Event Time Stamp Lower Bits	

TDC Data:

15..10	9..0
Channel #	Time Bits 1.18 ns steps

Event Status bits:

15..7	6	5	4	3	2	1	0

Not yet Defined	Ascii Link Parity Error	Command Link Parity Error	Word Count Overflow	Event FIFO Empty	Event FIFO Overflow	Trigger FIFO Overflow	Time Stamp Mismatch

Controller Time Stamp:

11..3	2..0
Lower order nine bits of controller 106.208MHz counter reset at spill begin	Time of arrival of trigger input w/r/t Controller 106.208MHz Counter 1.18ns steps

TDC Time Stamp:

0	15..0
	TDC 106.208MHz counter reset at spill begin bits 31..15
1	15..0
	TDC 106.208MHz counter reset at spill begin bits 15..0

Bit significance of the Time Stamps:

31..9	8..0
TDC Time Stamp Bits 31..0	

11..3	2..0
Controller Time Stamp Bits 11..0	

The TDC time stamp is the number of 9.4 ns clock ticks since begin spill. Assuming a five second spill, this word has at most 29 significant bits but is cast as a 32 bit quantity. The Controller time stamp is the lower order 12 bits of the number of 1.18ns ticks that have elapsed between begin spill until the receipt of this trigger. Bits 8..0 of the TDC time stamp are compared to bits 11..3 of the controller time stamp as a check of synchronization between the TDC and controller counters. The concatenation of the 32 bit TDC time stamp with the lower order three bits of the controller time stamp forms a 35 bit word which represents the time of arrival of the trigger with respect to spill begin in 1.18ns steps. The 10 bit TDC time word is a measure of the time elapsed from the trigger time stamp to the hit arrival in 1.18ns steps.

The absolute timing depends on (at least): The delay time in forming the trigger input to the controller, the time required by the controller to broadcast a trigger message to the TDCs (80 9.4 ns ticks), the cable delay between the controller and any given TDC, the delay from the wire chamber signal through the delay chain from ASDQ to the interior of the TDC FPGA. The pipeline delay adjustment delays the TDC hit data and is intended to align hit data with the trigger timing.