FTBF TDC operating parameters

The FTBF TDCs derive an RF clock from one of the two signals transmitted on the link from the controller. A TDC bin is defined as 1/16th of an RF bucket (1.177 ns). The TDC inputs consist of eight bit shift registers clocked at 849.6512 MHz. The parallel shift register outputs are priority encoded at a 106.2064 MHz rate to form the lower order three bits of the time word. This means that only one rising edge per 106 MHz clock tick can be recorded. There is a 64 bit register that can be used to disable any input in the event of a hot channel. A counter running at 106 MHz supplies the upper order bits of the time word. This counter can be preset to a value from -128 to +128 upon receipt of an Start Spill message from the controller. The desire is to synchronize the counter in the TDCs with the corresponding counter running in the controller. When synchronized, times associated with triggers in the controller and the TDCs can be cross checked, modulo cable delays.

A serial message is sent by the controller to the TDC in response to a NIM trigger pulse received at the controller LEMO input. This message consists of a four bit message ID field and 12 bits of time stamp. This ID is used to identify triggers of various types (e.g. normal and pulser). At a link bit rate of 26.55Mb/s, it takes 753ns to transmit a message, which means the maximum TDC trigger rate is limited to 1.33MHz. In order to align the hit data with the trigger messages coming from the controller, a pipeline delay adjustable in 9.4n steps is applied to the encoded hit data. The maximum delay is 256 steps.

In response to a trigger message, a gate generator in the TDC fires for a width defined by a seven bit register also with 9.4ns steps, so the widest gate is 1.196us. While this gate is high, any encoded hits emerging from the pipeline are written to a 256 deep first level buffer. At the same time, the value of a 32 bit 106MHz counter is latched and a seven bit counter also running at 106MHz is reset to zero. When a hit emerges from the pipeline within the gate, the value of the seven bit counter is used to form bits three through nine of the TDC word. To derive the time of a hit, add the TDC word time bits to the latched 32 bit counter value. At the end of the gate interval, a pivot routine is used to build channel ordered time words out of the time ordered data in the first level buffer. This process takes 604ns for each 9.4ns time slice that contains hits. Assuming that the most common occurrence is two to three slices with hits, a rate of 1.8us per trigger is the maximum sustained rate. The peak rate is the reciprocal of the gate width which in general I would assume is normally less than the 753ns limit above. The output of the pivot logic goes to a small staging FIFO for transfer to the DRAM. The bandwidth of the DRAM interface is 400Mbytes/s which is higher than the maximum scanner rate of 200Mbytes/s if there is a hit on every wire (e.g. a pulser event) so there should be no DRAM bottleneck. The DRAM is 64Mbytes so it cannot overflow, given the previously stated rate limits. The format of the time word is six bits of channel number and 10 bits of time value. Multiple hits on a channel will result in a channel number being repeated. The 1024 count span matches that of the maximum gate width.

TDC data is transferred to the controller at 2.6 Mbytes/s. The controller will spend some time concatenating the data from all the TDCs sending it data before sending the reformatted data to the experiment DAQ. At the very least a leading total word count will be tallied before sending Status information is included in the header appended to the data. The expected bandwidth of the Ethernet link is 6Mbytes/s shared by up to 16 TDCs. given a 50 second interspill, the largest data block that can be sent to the DAQ is 300Mbytes, so the system limit is the sustained trigger rate.