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FTBF TDC FPGA Register Map (word addresses)

0x00: Control and status register

Bit 0: Enable the TDC input pipeline

Bit 1: Enable TDC data write to the DDR

Bit 2: Reference source (read only)

0: no external reference, the VXO tuning voltage is set to the middle of its range.

1: the reference is the word link FM frequency

Bit 3: Enable DMA from the TDCs to the controller. 1: enabled, 0: disabled

Bit 4: Ignore Spill when taking triggers 1: Spill Ignored 0: Triggers gated by spill

Bit 5: Reset readout sequencer 1: Reset, 0: No action

Bit 6: Output Select 1: Out 0 is the TDC gate, 0: Out 0 is the “or” of the ASDQ inputs.

In either case, Out 1 is the pipeline delayed copy of the input hits.

Bits15:7: Not presently defined.

15..7	6	5	4	3	2	1	0
Not defined	Output Select	Reset Readout Sequencer	Ignore Spill Gate	DMA Enable	Reference Source	Enable DDR Writes	Pipeline Enable

0x01: Gate Width Register

Any data emerging from the hit pipeline that is in time with this gate gets written to the first level FIFO. The least count of the width setting is RF/2 (9.415 ns) and the span is seven bits, which corresponds to the time range of each TDC word.

0x02: Time stamp counter initial value

Upon receipt of a spill begin, a 32 bit counter running at 2∗RF is initialized to this value. It is a signed eight bit number (-128…+127). The desire is to have the time stamp counters in the controller and the TDCs synchronized.

0x03: Hit Pipeline Delay Register

Specifies the number of pipeline stages the hit data traverses before being presented to the first level FIFO. This is used to compensate for trigger delays. The least count is RF/2 and the span is eight bits. The minimum delay setting is one and increases monotonically up to a setting of 255. A setting of zero corresponds to a delay of 256 or 2.41μs.

0x04: TDC Channel Enable Bits 15...0

A one at a given bit position enables the ASDQ input, a zero disables it.

0x05: TDC Channel Enable Bits 31...16

A one at a given bit position enables the ASDQ input, a zero disables it.

0x06: TDC Channel Enable Bits 47...32

A one at a given bit position enables the ASDQ input, a zero disables it.

0x07: TDC Channel Enable Bits 63...48

A one at a given bit position enables the ASDQ input, a zero disables it.

0x08: Write Threshold DAC for ASDQ One

ASQD one is attached to input channels 0…7. The span of the 12 bit threshold DACs is 0 to +1.024 Volts.

0x09: Write Threshold DAC for ASDQ Two

ASQD two is attached to input channels 8…15.

0x0A: Write Threshold DAC for ASDQ Three

ASQD three is attached to input channels 16…23.

0x0B: Write Threshold DAC for ASDQ Four

ASQD four is attached to input channels 24…31.

0x0C: Write Threshold DAC for ASDQ Five

ASQD five is attached to input channels 32…39.

0x0D: Write Threshold DAC for ASDQ Six

ASQD six is attached to input channels 40…47.

0x0E: Write Threshold DAC for ASDQ Seven

ASQD seven is attached to input channels 48…55.

0x0F: Write Threshold DAC for ASDQ Eight

ASQD eight is attached to input channels 56…63.

0x10: Write IBLR DAC for all ASDQs

Set the base line restorer current adjustment. The span of the 12 bit DAC is 0 to +3 Volts.

0x11: Write TRefE DAC for all ASDQs

Sets the even channel test pulse magnitude. The span of the 12 bit DAC is -3 to +1.75 Volts.

0x12: Write TRefO DAC for all ASDQs

Sets the odd channel test pulse magnitude. The span of the 12 bit DAC is -3 to +1.75 Volts.

0x13: Unused DAC Channel

0x14: TDC Number

A five bit value that is written into the TDC number field in the event data header

0x15: Pulser trigger delay value

An eight bit value in steps of 9.4 ns that specifies the delay between receipt of a pulser trigger command from the controller and the issuing of a test pulse to the ASDQ chips. The desire is to obviate the need for pipeline readjustment between data taking and pulser triggers.

0x16: "OR" Out Channel Enable Bits 15...0

A one at a given bit position enables the ASDQ input, a zero disables it.

0x17: "OR" Out Channel Enable Bits 31...16

A one at a given bit position enables the ASDQ input, a zero disables it.

0x18: "OR" Out Channel Enable Bits 47...32

A one at a given bit position enables the ASDQ input, a zero disables it.

0x19: "OR" Out Channel Enable Bits 63...48

A one at a given bit position enables the ASDQ input, a zero disables it.

0x20: Link CSR register

Bits 1:0: Serial receiver parity error bits. A write of '1' to these positions will clear the error.

Bits 2: Byte Serial receiver buffer empty flag

Bits 3: Byte Serial receiver buffer full flag

Bits 4:5: Serial transmit buffer empty flags

15:6	5	4	3	2	1	0
Not used	Word Tx Buff Empty	Byte Tx Buff Empty	Byte Rx Buff Full	Byte Rx Buff Empty	Word Rx Parity Error	Byte Rx Parity Error

0x21: Link Interrupt register

Bit 0: A flags indicating a Null has been received on the byte link. A read of a null from the buffer FIFO will reset this flag. The flag is not buffered; the first null that is read, regardless of how many nulls were sent will clear the flag.

Bit 1: A flag indicating a carriage return has been received on the byte link. A read a carriage return from the buffer FIFO that shows will reset this flag. The flag is not buffered

Bit 2: A flag indicating an end of spill command has been received on the word link. Writing a one to this location or setting DMA enable will clear this flag.

Bit 2: One during the spill, zero during the interspill

15..3	3	2	1	0
Not defined	Spill Gate	End of Spill Received	CR Received	Null Char Received

0x22: Byte Link Read Port
0x23: Word Link Read Port
0x24: Byte Link Write Port
0x25: Word Link Write Port

0x26: DMA Word Count Register bits 31..16

A write to this register specifies the number of word to be transmitted from DRam to the word link when DMA enable is set.

0x27: DMA Word Count Register bits 15..0
0x28: SDRam data port bits 31..16
0x29: SDRam data port bits 15..0
0x2A: Set SDRam Read address upper bits

A write to this address defines bits the upper 9 bits of the SDRam read address

0x2B: Set SDRam Read address lower bits

A write to this address defines the lower 16 bits of the SDRam read address. At the end of this write cycle, the write address of the DPRam block attached to the SDRAM is reset, the specified address is applied to the SDRam and a burst read into the spooling DPRam is started.

0x2C: Set SDRam Write address upper bits

A write to this address defines the upper 9 bits of the SDRam read address

0x2D: Set SDRam Write address lower bits

A write to this address defines the lower 16 bits of the SDRam read address. After this, if there are at least 16 words in the input spooling FIFO, a burst of 16 words will start at the 25 bit address specified.

0x2E: Byte reversed version of 0x28
0x2F: Byte reversed version of 0x29

0x32: Read/Write upper byte of the Test Pulser frequency word

A write to this address defines the upper 16 bits of the test pulser repetition rate.

0x33: Read/Write lower word of the Test Pulser frequency word

A write to this address defines the lower 16 bits of the test pulser repetition rate. The rate is 0.0247 Hz per count.

0x34: Read the Spill Word Counter bits 31..16

Reads the number of TDC words accumulated during the spill.

0x35: Read the Spill Word Counter bits 15..0

0x36: Read the Spill Trigger Counter bits 31..16

Reads the number of triggers received during the spill

0x37: Read the Spill Trigger Counter bits 15..0

0x38: Read Gated Hit Counter

Reads the number of hits received during the spill within the trigger gate.

0x39: Read the Spill Status register

This register sets one bit for each attached TDC that had an error bit set in one or more of its status words.

Bit 0: Time stamp mismatch. Bits 11..3 of the controller time stamp do not match bits 8..0 of the TDC time stamp at some point during the spill.

Bit 1: The FIFO used as temporary storage of events while the first level of zero suppression is executed has overflowed.

Bit 2: The FIFO used as temporary storage of events while the second level of zero suppression is executed has overflowed..

Bit 2: The above FIFO is empty. This should be the case at the end of spill.

Bit 4: Parity error on the command link from the controller to the TDC.

Bit 5: One or more events during the spill exceeded 256 words in size.

7	6	5	4	3	2	1	0
Not yet Defined	Not yet Defined	Word Count Overflow	Command Link Parity Error	Event FIFO Empty	Event FIFO Overflow	Trigger FIFO Overflow	Time Stamp Mismatch

0x50: Read/Write test Counter Bits 31...16

A write to this address defines the upper 16 bits of the 32 bit test counter. A read returns the present value of the upper bits.

0x51: Read/Write test Counter Bits 15...0

A write to this address defines the lower 16 bits of the 32 bit test counter. A read from this address displays the value of the lower order bits and increments all 32 bits of the counter after the read.

0x52: Uptime Counter bits 31...16

0x53: Uptime Counter bits 15...0

A counter showing the number of seconds since the last FPGA reset

0x54: Read Word Count FIFO

If the DDR Ram writes are disabled, event word counts can be read from this FIFO.

0x55: Read the Event FIFO

If the DDR Ram writes are disabled, event data can be read from this FIFO.

0x56: Read the present value of the DMA down counter bits 31..16

If the DMA to the binary send port is in progress, the instantaneous value of the count is displayed. If the DMA is finished, the value is zero.

0x57: Read the present value of the DMA down counter bits 15..0