Sten Hansen 03/21/2014

FTBF TDC System Controller FPGA Register Map (word addresses)

0x01: Control and status register

Bit 0 DMA from the TDCs to the controller. 1: active, 0: inactive (read only)

Bit 1 0: no external reference, the VXO tuning voltage is set to the middle of its range. 1: the reference in the External Frequency/Beam Sync LEMO connector.

Bit 2: Enable the Send 2 FM transmitters 1: enabled, 0: disabled

Bit 3: Enable Test Pulser. 1: Enabled, 0: Disabled.

Bit 4: Test Pulser Single Step/ Free Run 1: One Spill. 0: Free Run

Bit 5: Reset the spill counter. 1: Counter is reset, 0: no action.

Bit 6: Reset the readout sequencer. 1: Sequencer is forced to Idle state. 0: no action.

Bit 7: Reset the link input FIFO buffers. 1: FIFOs are reset to empty. 0: not action.

Bits15:7: Not presently defined

15:8	7	6	5	4	3	2	1	0
Not Used	FIFO buffer Reset	Readout Sequencer Reset	Reset Spill Counter	Single Step/Free Run	Test Pulser Enable	Send 2 FM Tx Enable	PLL Reference Source	DMA Busy

0x02: Start Spill TClk Event Register The value in this register is compared to incoming TClk events. If there is a match, a Begin Spill command is issued to the TDCs and the controller readout sequencer is initialized.

0x03: End Spill TClk Event Register

The value in this register is compared to incoming TClk events. If there is a match, an End Spill command is issued to the TDCs and the controller readout sequencer starts to read out the TDCs.

0x04: Read the Spill Trigger Counter bits 31..16

Reads the number of triggers received during the spill. This counter is reset at begin spill.

0x05: Read the Spill Trigger Counter bits 15..0

0x06: Read the TDC Spill Status register

This register sets one bit for each attached TDC that had an error bit set in one or more of its status words.

0x07: Read the Spill Counter

This counter increments once for each begin spill. Bit 5 of the CSR resets this counter.

0x08: Read/Write Header Buffer Read Pointer

Read pointer. This is a 6 bit counter that increments once for each Header Buffer read.

0x09: Header Buffer Data port

There is a 64 deep dual port memory containing the spill headers from all attached TDCs.

A read from this port displays on header word and increments the Header Buffer Read Pointer. There are four spill header words per TDC.

0x0A: Header Buffer Write Pointer (read only)

This is a 6 bit counter that increments once for each Header Buffer write. The writes are done by the readout sequencer.

0x0B: Spill State Register (read only)

Bit 0: DMA from the TDCs to the controller in progress. 1: active, 0: inactive
Bit 1: DMA from the TDCs to the controller done. 1: done, 0: active
Bit 2: EOT Received from all connected TDCs
Bit 3: Spill Gate. 1: Spill. 0: Interspill.

15..4	3	2	1	0
Not yet defined	Spill Gate	EOT Received from all TDCs	TDC Readout Done	TDC Readout Busy

0x0C: Link Activity Register (read only)

This register displays the number of TDCs attached to the controller. Bits 0…15 indicate TDC port 1…16.

0x0E: Scratch Pad High

This register is intended for use by the microcontroller for storing the spill word count bits 31...16.

0x0F: Scratch Pad Low

This register is intended for use by the microcontroller for storing the spill word count bits 15…0.

0x10...0x1F: Read the DMA word counts associated with the 16 TDC data ports.

Address 0x10 reads port 1, address 0x1F reads port 16.

0x20...0x2F: TDC port Link CSR registers

Address 0x20 reads port 1, address 0x2F reads port 16.

Bits 1:0: Serial receiver parity error bits. A write of '1' to these positions will clear the error.
Bits 3:2: Serial receiver buffer empty flags
Bits 5:4: Serial receiver buffer full flags
Bit 6: Serial transmit buffer empty
Bit 7: Serial transmit buffer full

15:7	7	6	5	4	3	2	1	0
Not yet defined	Byte Tx Buff Full	Byte Tx Buff Empty	Word Rx Buff Full	Byte Rx Buff Full	Word Rx Buff Empty	Byte Rx Buff Empty	Word Rx Parity Error	Byte Rx Parity Error

0x30...0x3F: TDC port Interrupt Status registers

Address 0x20 reads port 1, address 0x2F reads port 16.

Bit 0: A flags indicating a Null has been received on the byte link. A read of a null from the buffer FIFO will reset this flag. The flag is not buffered; the first null that is read, regardless of how many nulls were sent will clear the flag.

Bit 1: A flag indicating a carriage return has been received on the byte link. A read a carriage return from the buffer FIFO that shows will reset this flag. The flag is not buffered

Bit 2: A flags indicating an end of transmission (EOT) has been received on the byte link. A write of a '1' to bit position 2 clears the set bit. This character is not written into the receive buffer, therefore reading the buffer cannot be used to clear the flag.

15..3	2	1	0
Not yet defined	EOT	CR Received	Null Char Received

0x40...0x4F: Byte Receive Ports

Address 0x40 reads port 1, address 0x4F reads port 16.

0x50...0x5F: Word Receive Ports

Address 0x50 reads port 1, address 0x5F reads port 16.

0x60...0x6F: Byte Transmit Ports

Address 0x60 writes port 1, address 0x5F writes port 16.

0x70: Broadcast word transmit

A write to this address sends a word to all 16 word transmit ports

0x71: Broadcast byte transmit

A write to this address sends a word to all 16 byte transmit ports

0x72: SDRam data port bits 31..16

0x73: SDRam data port bits 15..0

0x74: Set SDRam Read address upper bits

A write to this address defines the upper 9 bits of the SDRam read address

0x75: Set SDRam Read address lower bits

A write to this address defines the lower 16 bits of the SDRam read address. At the end of this write cycle, the write address of the DPRam block attached to the SDRAM is reset, the specified address is applied to the SDRam and a burst read into the spooling DPRam is started.

0x76: Set SDRam Write address upper bits

A write to this address defines the upper 9 bits of the SDRam read address

0x77: Set SDRam Write address lower bits

A write to this address defines the lower 16 bits of the SDRam read address. If there are at least 16 words in the input spooling FIFO, a burst of 16 words will start at the 25 bit address specified.

0x7A: SDRam byte swapped data port bits 31..16 (Bits 23..16,31..24)

0x7B: SDRam byte swapped data port bits 15..0 (Bits 7..0,15..8)

0x7C: Read/Write upper byte of the Test Pulser frequency word

A write to this address defines bits the upper 16 bits of the test pulser repetition rate.

0x7D: Read/Write lower word of the Test Pulser frequency word

A write to this address defines bits the lower 16 bits of the test pulser repetition rate. The rate is 0.0247 Hz per count.

0x7E: Read/Write internally generated spill gate width

A write to this address defines the length of the internally generated spill gate in seconds.

0x7F: Read/Write internally generated inter-spill interval

A write to this address defines the length of the internally generated inter-spill interval in seconds.

0x80: Read/Write test Counter Bits 31...16

A write to this address defines the upper 16 bits of the 32 bit test counter. A read returns the present value of the upper bits.

0x81: Read/Write test Counter Bits 15...0

A write to this address defines the lower 16 bits of the 32 bit test counter. A read from this address displays the value of the lower order bits and increments all 32 bits of the counter after the read.

0x86: Uptime Counter bits 31...16

0x87: Uptime Counter bits 15...0

A counter showing the number of seconds since the last FPGA reset

0x88: Trigger Inhibit register

Bit 0: A bit indicating that triggers are inhibited. 1: Triggers Inhibited; 0: Triggers enabled. This bit is reset to zero upon receipt of end spill.

Bit 1: A bit indicating that bit 0 is significant. 1: Bit 0 controls triggers; 0: Bit 0 ignored.

15..2	1	0
Not yet defined	Trig Inhibit Enabled	Trig Inhibit

0x89: Read the trigger time stamp

The time at which each of the first 2048 triggers occurred is stored in this FIFO.