125MHz Digitizer Firmware version ABB0F (PXIE and MI Toroids)

Note: changes from version ABB0E:

Change the size of Gate Width register:			
Register	**Address**	**Data Width**	**Default Value (Hex)**
Gate Size	0x21C	32	Read only.

Integration Readout and Threshold Settings are 40 Bits saved in two registers		
	Upper 8 bits	Lower 32 bits
Integration:	Bits 39 – Bit 32	Bits 31 ---------- Bit 0
Threshold:	Bits 39 – Bit 32	Bits 31 ---------- Bit 0

Intensity Readout (Corrected) – Upper 8 Bits		
Register	**Add.**	**Data Width**
INT Channel 1	0x318	8
INT Channel 2	0x319	8
INT Channel 3	0x31A	8
INT Channel 4	0x31B	8
INT Channel 5	0x31C	8
INT Channel 6	0x31D	8
INT Channel 7	0x31E	8
INT Channel 8	0x31F	8

Intensity Readout (Corrected) – Lower 32 Bits		
Register	**Add.**	**Data Width**
INT Channel 1	0x3D0	32
INT Channel 2	0x3D4	32
INT Channel 3	0x3D8	32
INT Channel 4	0x3DC	32
INT Channel 5	0x3E0	32
INT Channel 6	0x3E4	32
INT Channel 7	0x3E8	32
INT Channel 8	0x3EC	32

Pulse Only Integration Readout – Upper 8 Bits		
Register	**Add.**	**Data Width**
Pulse Channel 1	0x308	8
Pulse Channel 2	0x309	8
Pulse Channel 3	0x30A	8
Pulse Channel 4	0x30B	8
Pulse Channel 5	0x30C	8
Pulse Channel 6	0x30D	8
Pulse Channel 7	0x30E	8
Pulse Channel 8	0x30F	8

Pulse Only Integration Readout – Lower 32 Bits		
Register	**Add.**	**Data Width**
Pulse Channel 1	0x380	32
Pulse Channel 2	0x384	32
Pulse Channel 3	0x388	32
Pulse Channel 4	0x38C	32
Pulse Channel 5	0x390	32
Pulse Channel 6	0x394	32
Pulse Channel 7	0x398	32
Pulse Channel 8	0x39C	32

Baseline Integration Readout – Upper 8 Bits		
Register	**Add.**	**Data Width**
Baseline Channel 1	0x310	8
Baseline Channel 2	0x311	8
Baseline Channel 3	0x312	8
Baseline Channel 4	0x313	8
Baseline Channel 5	0x314	8
Baseline Channel 6	0x315	8
Baseline Channel 7	0x316	8
Baseline Channel 8	0x317	8

Baseline Integration Readout – Lower 32 Bits		
Register	**Add.**	**Data Width**
Baseline Channel 1	0x3A0	32
Baseline Channel 2	0x3A4	32
Baseline Channel 3	0x3A8	32
Baseline Channel 4	0x3AC	32
Baseline Channel 5	0x3B0	32
Baseline Channel 6	0x3B4	32
Baseline Channel 7	0x3B8	32
Baseline Channel 8	0x3BC	32

Machine Protection Thresholds – Upper 8 Bits		
Register	**Add.**	**D. Width**
Upper Threshold Ch1	0x360	8
Upper Threshold Ch2	0x361	8
Upper Threshold Ch3	0x362	8
Upper Threshold Ch4	0x363	8
Upper Threshold Ch5	0x364	8
Upper Threshold Ch6	0x365	8
Upper Threshold Ch7	0x366	8
Upper Threshold Ch8	0x367	8

Machine Protection Thresholds – Lower 32 Bits		
Register	**Add.**	**D. Width**
Upper Threshold Ch1	0x320	32
Upper Threshold Ch2	0x324	32
Upper Threshold Ch3	0x328	32
Upper Threshold Ch4	0x32C	32
Upper Threshold Ch5	0x330	32
Upper Threshold Ch6	0x334	32
Upper Threshold Ch7	0x338	32
Upper Threshold Ch8	0x33C	32

Machine Protection Thresholds - Upper 8 Bits		
Register	**Add.**	**D. Width**
Lower Threshold Ch1	0x368	8
Lower Threshold Ch2	0x369	8
Lower Threshold Ch3	0x36A	8
Lower Threshold Ch4	0x36B	8
Lower Threshold Ch5	0x36C	8
Lower Threshold Ch6	0x36D	8
Lower Threshold Ch7	0x36E	8
Lower Threshold Ch8	0x36F	8

Machine Protection – Lower 32 Bits		
Register	**Add.**	**D. Width**
Lower Threshold Ch1	0x340	32
Lower Threshold Ch2	0x344	32
Lower Threshold Ch3	0x348	32
Lower Threshold Ch4	0x34C	32
Lower Threshold Ch5	0x350	32
Lower Threshold Ch6	0x354	32
Lower Threshold Ch7	0x358	32
Lower Threshold Ch8	0x35C	32