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VRFT-VUCD preliminary

Recipe to get pattern generator to play

Write pattern to waveform memory beginning at offset 0x40000 ending at 0x4FFFC.
Write TCLOCK event(s) to memory beginning at offset 0x00000 ending at 0x007FC.
Write BSYC event to memory beginning at offset 0x08000 ending at 0x087fc.
Write to trigger mux at offset 0x2002C.
Write beginning pattern generator address to offset 0x20040.
Write ending pattern generator address to offset 0x20044.
Write lap-count to offset 0x20048.
Write to offset 0x20050, data 0x01 to enable pattern generator.
Write to offset 0x10440, data 0x01 to enable TCLOCK decoder.
Write to offset 0x10440, data 0x03 to enable BSYNC decoder.
Write to offset beginning at 0x10200 to set up 8-bit VME type interrupt.
Write to offset beginning at 0x10220 to choose interrupt source.
Write to offset 0x10240 to set up 16-bit VXI type interrupt status/ID
Write to offset 0x10260 to select VME/VXI interrupt type: 0 = VME. 1 = VXI.
Write to offset 0x20100 to set delay after event.
Write to offset 0x20034 to select 1 of 8 STOP source.

Note: There is no special order or sequence required for programming the register or memory locations. Enabling the pattern generator would sensibly be the last thing to do but it is not essential. Enabling the pattern generator prior to having all other parts of the module programmed could momentarily produce unintended trigger(s).

<u>Example terminal commands</u>
Write pattern to waveform memory beginning at 0x40000

```
->m 0xfad40000,4
fad40000:  00000000-00
fad40004:  00000000-ff
fad40008:  00000000-ff
fad4000c:  00000000-ff
fad40010:  00000000-ff
fad40014:  00000000-ff
fad40018:  00000000-ff
fad4001c:  00000000-ff
fad40020:  00000000-ff
fad40024:  00000000-ff
fad40028:  00000000-ff
fad4002c:  00000000-ff
fad40030:  00000000-ff
```

fad40034: 00000000-ff
fad40038: 00000000-ff
fad4003c: 00000000-ff
fad40040: 00000000-ff
fad40044: 00000000-ff
fad40048: 00000000-ff
fad4004c: 00000000-ff
fad40050: 00000000-ff
fad40054: 00000000-00
…
fad7fffc: 00000000-00
fad80000: 00000000-.

Write TCLOCK event(s) to memory beginning at 0x00000; in this example detect only event TCLOCK 0x02 on column zero only.
->m 0xfad00000
fad00000: 00000000-00
fad00004: 00000000-00
fad00008: 00000000-01
fad0000c: 00000000-00
...
fad003fc: 00000000-00
fad00400: 00000000-.

Write BSYC event to memory beginning at 0x08000; in this example set bits to detect only event BSYNC 0xAA on column zero only.
->m 0xfad082a8
fad08000: 00000000-00
fad08004: 00000000-00
...
fad082a8: 00000000-01
fad082ac: 00000000-00
…
fad083fc: 00000000-00
fad08400: 00000000-.

Write to trigger mux at offset 0x2002C; in this example set trig mux to “trigger pattern generator on first BSYC 0xAA after TCLOCK 0x02”.
->m 0xfad2002c
fad2002c: 00000000-3
fad20030: 00000000-
fad20034: 00000000-
fad20038: 00000000-
fad2003c: 00000000-.

Write beginning pattern generator address to offset 0x20040; in this example the beginning address would be 0x01.
fad20040: 00000000-01
fad20044: 00000000-.

Write end pattern generator address to offset 0x20044; in this example the end address would be 0x16.
fad20044: 00000000-16

Write the required laps offset 0x20048; in this example the lap count would 0 (zero). In this case the pattern plays only once.
fad20048: 00000000-0
fad2004c: 00000000-.

Write to offset 0x20050, data 0x01, to enable pattern generator.
fad20050: 00000000-1
fad20054: 00000000-.

Write to control register, offset 0x10440 to enable serial clocks
->m 0xfad10440
fad10440: 00000000-01 - enable BSYNC decoder
fad10444: 00000000-.
->m 0xfad10440
fad10440: 00000000-03 - enable TCLOCK decoder
fad10444: 00000000-.

Write to offset beginning at 0x10200 to set up 8-bit VME type interrupt
->m 0xfad10200
fad10200: 00000000-11aa - enable interrupt on control register 0, level-1,vector-0xAA
fad10204: 00000000-.

Write to offset beginning at 0x10220 to point interrupt source to column-1, TCLOCK memory
fad10220: 00000001- 01
fad10224: 00000001-.
Note: During VME type interrupt acknowledge cycle an 8-bit vector will be returned.

Write to offset 0x10240 to set up 16-bit VXI type interrupt status/ID
->m 0xfad10240
fad10240: 00000000-FDXX - write status/ID
Note: During VXI type interrupt acknowledge cycle, an 16-bit status/ID will be returned.

Write to offset 0x10260 to select VME/VXI interrupt type: 0 = VME. 1 = VXI
->m 0xfad10260
fad10200: 00000000-0001 - enable VXI mode interrupt

Write to offset 0x20000 to set delay, in increments of 100ns, between TCLOCK trigger and PPG trigger.
->m 0xfad20000
fad20100: 00000000-1000
fad20104: 00000000-.

Write to offset 0x20034 to select 1 of 8 STOP source. Set to ZERO to deselect STOP. Once a STOP event occurs, the PPG RAM needs to be re-enabled before a pattern will again play.
->m 0xfad20034
fad20010: 00000000-2

STATUS

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TRIGGER SELECTI4	TRIGGER SELECTI3	TRIGGER SELECTI2	TRIGGER SELECTI1	TRIGGER SELECTI0					Stop		Triggered		PPG Trigger	RF Present	RF Source
D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
														7.5mhz locked	Clock DELAY

Address Base + offset +	Register	Data							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
$00	CR0	F	FAC	X/IN	IRE	IRAC	L2	L1	L0
$04	CR1	F	FAC	X/IN	IRE	IRAC	L2	L1	L0
$08	CR2	F	FAC	X/IN	IRE	IRAC	L2	L1	L0
$0C	CR3	F	FAC	X/IN	IRE	IRAC	L2	L1	L0
$10	VR0	V7	V6	V5	V4	V3	V2	V1	V0
$14	VR1	V7	V6	V5	V4	V3	V2	V1	V0
$18	VR2	V7	V6	V5	V4	V3	V2	V1	V0
$1C	VR3	V7	V6	V5	V4	V3	V2	V1	V0

- CR0-CR3 - Control register
- VR3-VR0 - Vector register
- F - User Flag
- FAC - Flag auto clear
- X/IN - External/Internal vector
- IRE - Interrupt enable
- IRAC - Interrupt enable auto clear

- L2-L0 - Interrupt level
- V7-V0 - Vector data