

# Register Description for 16 Channel 80MHz Board for CMTF Interlock

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This is a quick description for reading out raw ADC data using the IPM firmware. I haven't understood the firmware well enough to write a complete documentation. But these registers will be enough for these tasks now. Later on when I make modifications for a more complete version, these registers will stay the same.

Register	Address	Width	Description
<b>Data Pointer to Raw</b>	0x4	32	A32 Data pointer for raw data.
<b>Data Size for Raw</b>	0x8	32	Buffer size (number of 4-byte words) for raw data (All 16 channels together).  At this point, "per channel buffer size" is fixed at 0x20000 bytes per channel. This is determined by part of the code in NIOS, I haven't figured out the exact relationship, but for now, we are going to have to take the default 0x20000 bytes per channel buffer (this limits raw data to 0x10000 samples per channel). Therefore this register has to be set at a minimum of 0x80000. Setting it over 0x80000 won't do much, but setting it under 0x80000 would make unavailable data from the last channel, or channels.
<b>Mode</b>	0x120	8	Digitizer Run Mode. 0x0: Trigger Mode with software arm. 0x1: Trigger Mode with External arm. 0x2: Trigger Mode with software arm and External gate. 0x3: Trigger Mode with external arm and external gate. <b>0x4: Scope Mode with software arm.</b> <b>0x5: Scope Mode with external arm.</b> 0x6: Scope Mode with software arm and external gate. 0x7: Scope Mode with External arm and External gate. 0x8, 0x9: IPM modes.
<b>Mode Run</b>	0x121	8	Set to "1" to arm (software arm) digitizer to run under specified mode.
<b>Mode Reset</b>	0x122	8	Write anything to reset digitizer back to Idle state.
<b>Number of Triggers</b>	0xF4	32	Number of triggers for Trigger modes
<b>Trigger Count</b>	0xF8	32	Read Only. Current trigger count.
<b>Number of Samples</b>	0xFC	32	Number of Samples to read for Scope modes, or Number of Sample per Trigger for Trigger modes.
<b>Sample Count</b>	0x100	32	Read Only. Current sample count.
<b>Mon Out</b>	0xD5	8	Mon. Out output source. 0x0: Sync In, 0x1: Trigger, 0x2: Gate, 0x3 TCLK Start, 0x4: TCLK Stop, 0x5: BSYNC Start, 0x6: BSYNC Stop, 0x7: ADC Clock.

**Clock Register Values:**

<b>Register</b>	<b>Address</b>	<b>Width</b>	<b>Internal (62.5MHz)</b>	<b>External (Requires clock input)</b>
<b>Reg0</b>	0x0	32	0x8180002	0x8146022
<b>Reg1</b>	0x4	32	0x8180002	0x8146022
<b>Reg2</b>	0x8	32	0x8180000	0x8146020
<b>Reg3</b>	0xC	32	0x8080000	0x6486030
<b>Reg4</b>	0x10	32	0x8080001	0x6486031
<b>Reg5</b>	0x14	32	0x11F40AE	0x10A40BE
<b>Reg6</b>	0x18	32	0x04BE49C	0x04BE198
<b>Reg7</b>	0x1C	32	0xBD0037F	0xBD0037F
<b>Reg8</b>	0x20	32	0x20009CF	0x20009BF