

125MHz Digitizer Firmware version ABB06 (Main Injector and Recycler Toroids)

Note: changes from version ABB01:

Initialize the registers as follows:			
Register	Address	Data Width	Default Value (Hex)
Digitizer Mode	0x200	8	0x88
A32 Data Pointer	0x04	32	You decide.
Channel Buffer Size	0x08	32	0x10000
Number of Raw Samples	0x20C	32	0x2000
Window Size	0x2BA	16	0x800
Sync Delay	0x2C0	16	0x0
Baseline Average Size	0x3C1	8	0x3
Polarity Flip	0x3C2	8	0xFF
Baseline Correction	0x3C3	8	0xFF

Added Readout Registers (Read Only)			
Register	Add.	Data Width	Description
FFT Scaling Factor Ch1	0x3C4	8	FFT Mag. = RAM Data * 2 ^ (-X)
FFT Scaling Factor Ch2	0x3C5	8	FFT Mag. = RAM Data * 2 ^ (-X)
FFT Scaling Factor Ch3	0x3C6	8	FFT Mag. = RAM Data * 2 ^ (-X)
FFT Scaling Factor Ch4	0x3C7	8	FFT Mag. = RAM Data * 2 ^ (-X)
FFT Scaling Factor Ch5	0x3C8	8	FFT Mag. = RAM Data * 2 ^ (-X)
FFT Scaling Factor Ch6	0x3C9	8	FFT Mag. = RAM Data * 2 ^ (-X)
FFT Scaling Factor Ch7	0x3CA	8	FFT Mag. = RAM Data * 2 ^ (-X)
FFT Scaling Factor Ch8	0x3CB	8	FFT Mag. = RAM Data * 2 ^ (-X)
Gate Size	0x21C	16	Length of the "Gate" input. Unit: clock cycles.

Clock Register Default Values (125MHz)	
Address	Default Value
A0	0x8146002
A4	0x8146002
A8	0x8146000
AC	0x6486030
B0	0x6486031
B4	0x10F00BE
B8	0x04B2030
BC	0xBD0037F
C0	0x20009F5

New readout devices to be created (FOR EACH EXISTING TOROID):	
1	FFT (corrected with scaling factor)
2	Gate Size (?)

125MHz Digitizer Firmware Description

Version: ABB06 (For Main Injector and Recycler Toroids)

1. Hardware: the digitizer

6U VME Board

8 Channel analog input, 14 bit ADC (ADS6445), $F_s(\max) = 125\text{MSPS}$

DC coupling with 2-stage ADA4927 Pre-Amp

Cyclone III FPGA handles data processing

16Msamples per channel buffer on DDR2 SDRAM

CDCE62005 clock chip with onboard 125MHz oscillator and external clock input

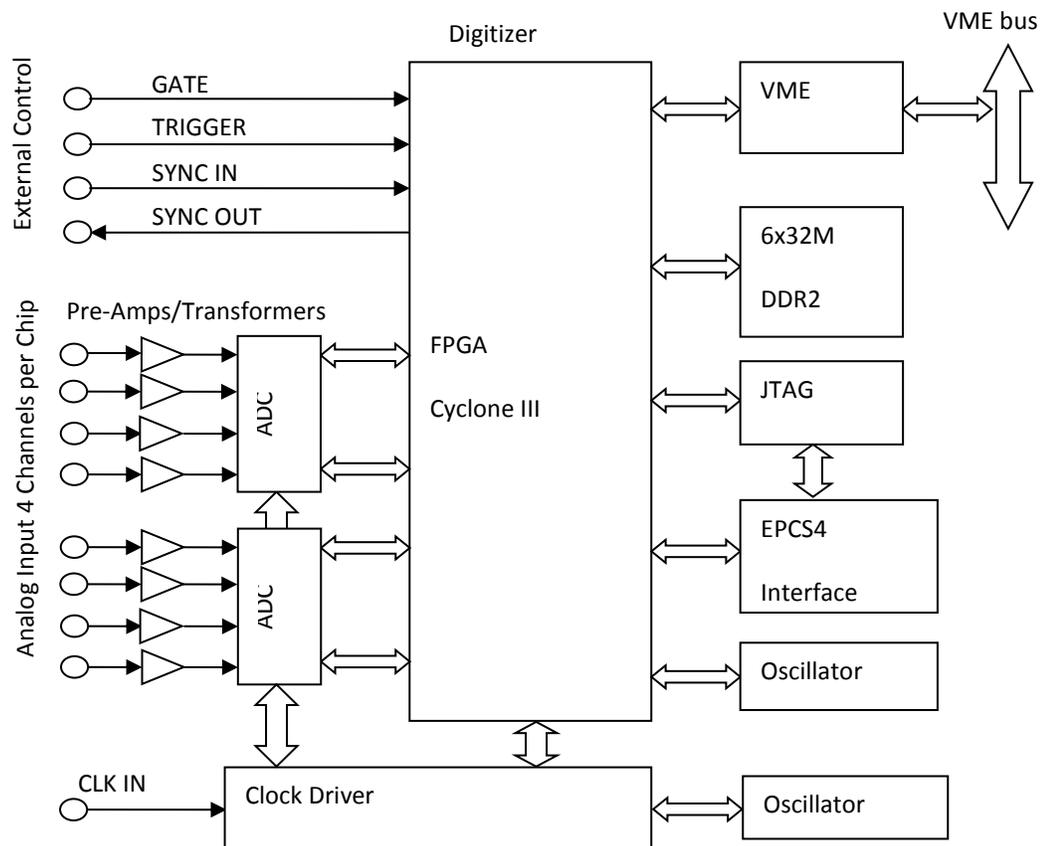
Three (3) additional digital inputs for smart triggering

One (1) digital output (programmable)

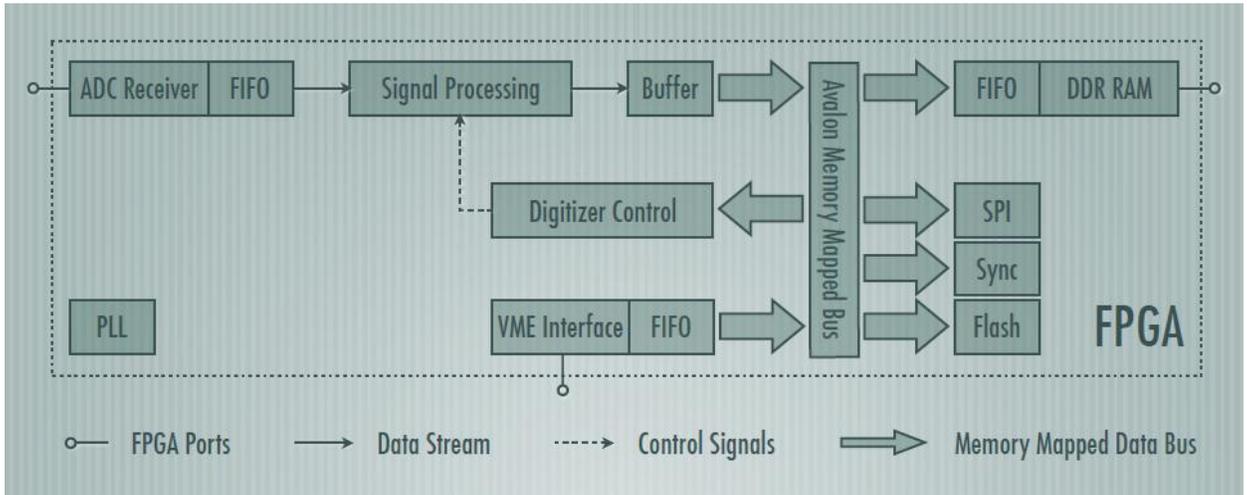
Draws 2.5A of current



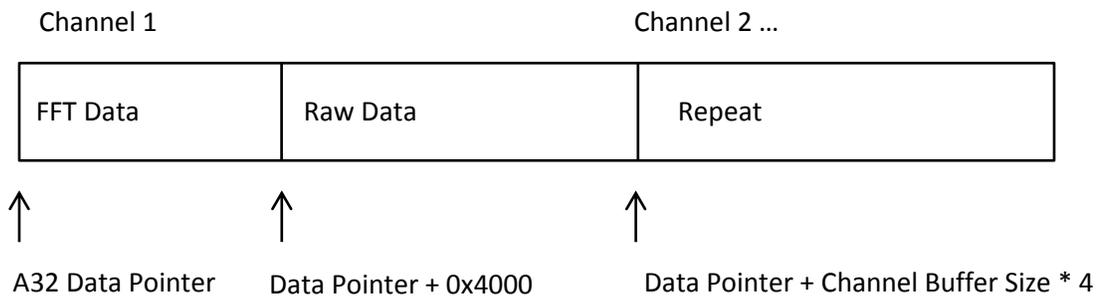
Digitizer Hardware Block Diagram:



2. Firmware Block Diagram



3. Address Map



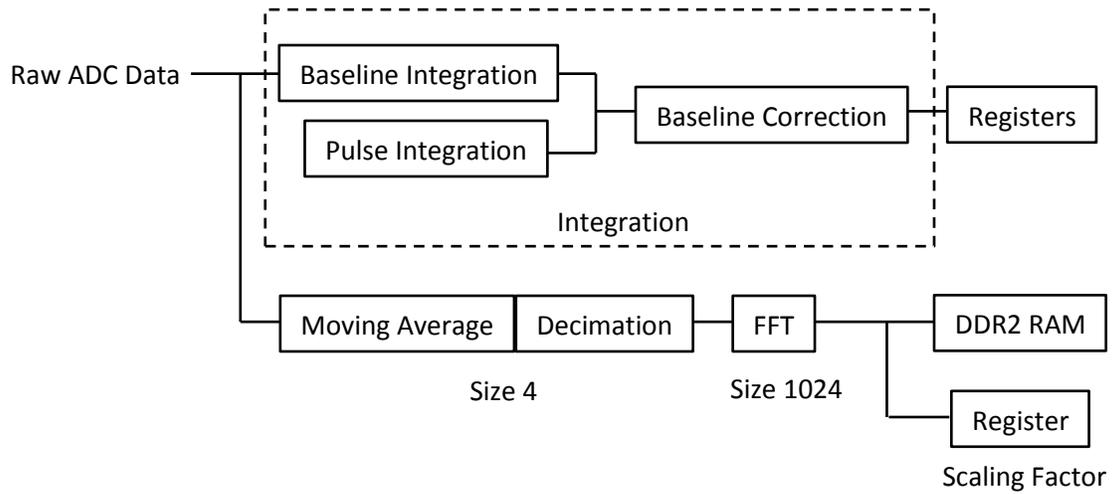
Memory location for FFT data = Data Pointer + (CH# - 1) * Buffer Size * 4. This part of memory is not used in this design.

For example, with default settings, channel 1 starts at 0x8000000, with channel buffer size set at "0x10000", channel 2 starts at 0x8040000, etc.

Raw data are stored in the channel's memory block after the FFT data. Address offset is x4000.

All registers are in A16 address space with an offset set by the Hardware Address Switches. All addresses can be accessed in 8, 16 or 32 bits.

4. Signal Processing



Note that FFT window starts right after Sync Delay.

5. Pulse Current and Intensity Calculation Using the FFT method:

The calculations here are tentative and will be discussed and revised if necessary.

S = FFT Scaling Factor

$F(n)$ = FFT Data, index start from 0 to 1023

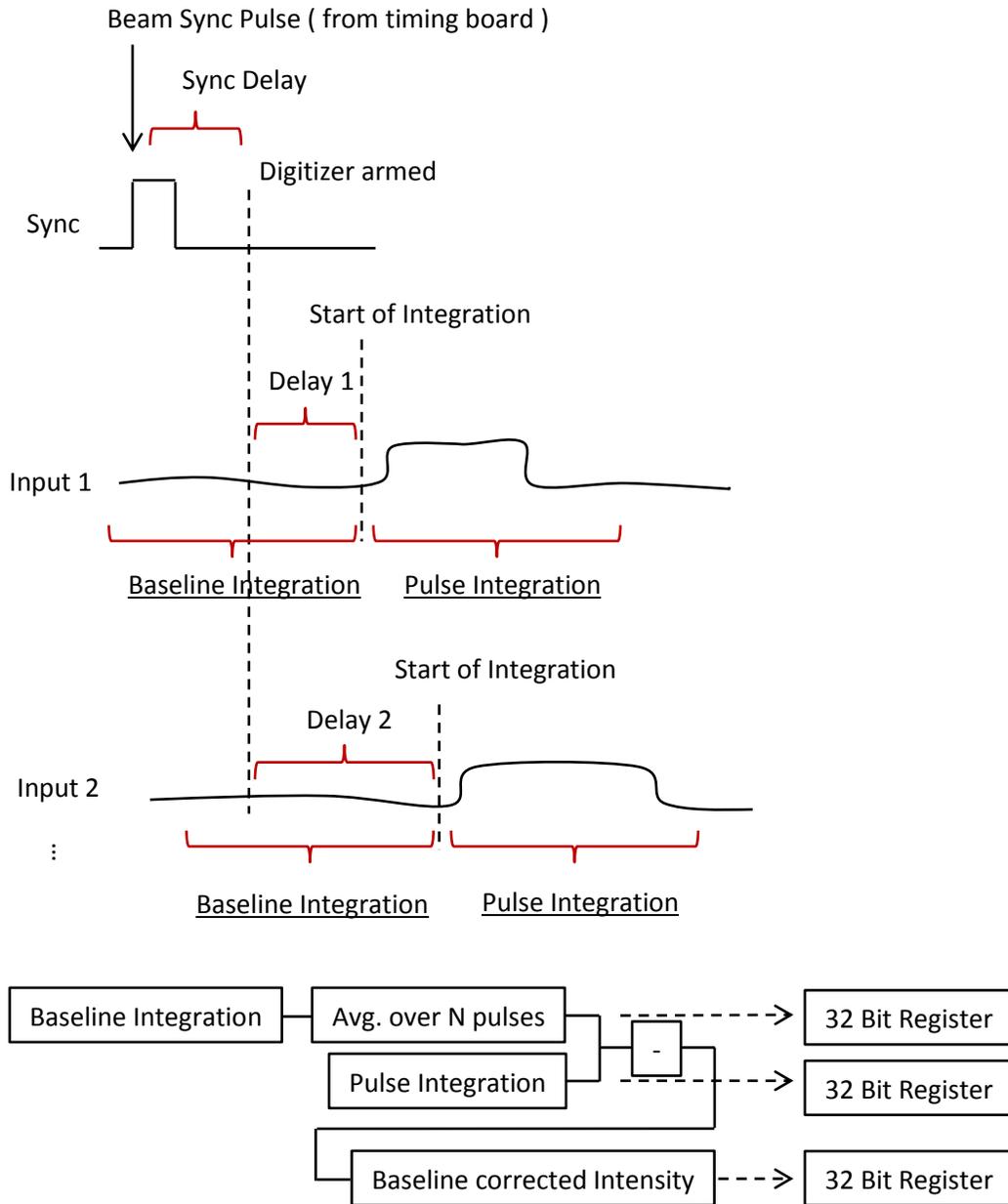
$FI(n)$ = FFT Data of an ideal pulse, index start from 0 to 1023

$$\text{Pulse current reading} = \sum (F(n) * 2^{(-S)} * FI(n)), 3 \leq n \leq 511$$

G = Gate size (length of the Gate pulse input which is in sync with beam pulse)

$$\text{Pulse Intensity reading} = \text{Pulse current reading} * G$$

6. Integration of Beam Pulse



Baseline and Pulse integration window size are set by the same register. Baseline integration uses buffer data points, maximum size 8192. Integrated Baseline is averaged "Pulse-Over-Pulse", by default over 8 pulses, 128 max.

All register values will be available at the time the last integration window is finished, and will stay available until the digitizer receives the next sync pulse.

7. Register description

Key Registers

Register	Add.	Data Width	Description
Digitizer Mode	0x200	8	Use x88. Bit <7> - '1' - External (Sync) arm, '0' - software arm. Bit <6> - '1' - Sample on trigger, '0' - no trigger. Bit <5> - '1' - Use gate, '0' - no gate. Bits <3:2> - Use "10" for Integration mode.
Switch Off	0x201	8	Write '1' to force digitizer to stop.
Software Arm	0x203	8	Set to '1' to arm.
Digitizer Busy	0x2AE	8	Read only. '1' - Busy, '0' - Not busy.
Firmware Version	0x2A8	32	Read only. Shows firmware version.
Block Count	0x218	32	Read only. Number of runs.
A32 Data Pointer	0x04	32	Address offset for corrected data. To access ADC raw data use Data Pointer + x4000 as address.
Channel Buffer Size	0x08	32	Number of 32-bit words reserved for each channel in the memory.
Raw Data Sampling Rate	0x204	16	Bits <15:0> - Hex value is the sampling rate factor. $T_s = T_c * (VALUE + 1)$, where $T_c = 1/clock_rate$.
Number of Raw Samples	0x20C	32	Bits <23:0> - Number of samples or Number of Samples Per Trigger in trigger modes.
Window Size	0x2BA	16	Integration window size (in sample counts) for both Pulse and Baseline.
Sync Delay	0x2C0	16	Delay of # ADC-clock cycles after digitizer receives trigger.
Channel Delay 1	0x3F0	16	Number of clock cycles delayed after digitizer is armed, before integration begins. Channel 1
Channel Delay 2	0x3F2	16	Number of clock cycles delayed after digitizer is armed, before integration begins. Channel 2
Channel Delay 3	0x3F4	16	Number of clock cycles delayed after digitizer is armed, before integration begins. Channel 3
Channel Delay 4	0x3F6	16	Number of clock cycles delayed after digitizer is armed, before integration begins. Channel 4
Channel Delay 5	0x3F8	16	Number of clock cycles delayed after digitizer is armed, before integration begins. Channel 5
Channel Delay 6	0x3FA	16	Number of clock cycles delayed after digitizer is armed, before integration begins. Channel 6
Channel Delay 7	0x3FC	16	Number of clock cycles delayed after digitizer is armed, before integration begins. Channel 7
Channel Delay 8	0x3FE	16	Number of clock cycles delayed after digitizer is armed, before integration begins. Channel 8
Baseline Average Size	0x3C1	8	Size of Baseline Pulse-Over-Pulse Averaging, max 128
Polarity Flip	0x3C2	8	Flip polarity of Intensity reading. Bits <7:0> - Ch8 - 1. '0' - Flip, '1' - Don't flip.
Baseline Correction	0x3C3	8	Bits <7:0> - Ch8 - 1. '1' = ON, '0' = OFF.

Intensity Readout (Read Only)			
Register	Add.	Data Width	Description
INT Channel 1	0x3D0	32	Baseline corrected Pulse Integration. Channel 1.
INT Channel 2	0x3D4	32	Baseline corrected Pulse Integration. Channel 2.
INT Channel 3	0x3D8	32	Baseline corrected Pulse Integration. Channel 3.
INT Channel 4	0x3DC	32	Baseline corrected Pulse Integration. Channel 4.
INT Channel 5	0x3E0	32	Baseline corrected Pulse Integration. Channel 5.
INT Channel 6	0x3E4	32	Baseline corrected Pulse Integration. Channel 6.
INT Channel 7	0x3E8	32	Baseline corrected Pulse Integration. Channel 7.
INT Channel 8	0x3EC	32	Baseline corrected Pulse Integration. Channel 8.

Pulse Only Integration Readout (Read Only)			
Register	Add.	Data Width	Description
Pulse Channel 1	0x380	32	Pulse Integration (Pulse only). Channel 1.
Pulse Channel 2	0x384	32	Pulse Integration (Pulse only). Channel 2.
Pulse Channel 3	0x388	32	Pulse Integration (Pulse only). Channel 3.
Pulse Channel 4	0x38C	32	Pulse Integration (Pulse only). Channel 4.
Pulse Channel 5	0x390	32	Pulse Integration (Pulse only). Channel 5.
Pulse Channel 6	0x394	32	Pulse Integration (Pulse only). Channel 6.
Pulse Channel 7	0x398	32	Pulse Integration (Pulse only). Channel 7.
Pulse Channel 8	0x39C	32	Pulse Integration (Pulse only). Channel 8.

Baseline Integration Readout (Read Only)			
Register	Add.	Data Width	Description
Baseline Channel 1	0x3A0	32	Baseline Integration, averaged. Channel 1.
Baseline Channel 2	0x3A4	32	Baseline Integration, averaged. Channel 2.
Baseline Channel 3	0x3A8	32	Baseline Integration, averaged. Channel 3.
Baseline Channel 4	0x3AC	32	Baseline Integration, averaged. Channel 4.
Baseline Channel 5	0x3B0	32	Baseline Integration, averaged. Channel 5.
Baseline Channel 6	0x3B4	32	Baseline Integration, averaged. Channel 6.
Baseline Channel 7	0x3B8	32	Baseline Integration, averaged. Channel 7.
Baseline Channel 8	0x3BC	32	Baseline Integration, averaged. Channel 8.

FFT Related (Read Only)			
Register	Add.	Data Width	Description

FFT Scaling Factor Ch1	0x3C4	8	FFT Mag. = RAM Data * 2 ^ (-X)
FFT Scaling Factor Ch2	0x3C5	8	FFT Mag. = RAM Data * 2 ^ (-X)
FFT Scaling Factor Ch3	0x3C6	8	FFT Mag. = RAM Data * 2 ^ (-X)
FFT Scaling Factor Ch4	0x3C7	8	FFT Mag. = RAM Data * 2 ^ (-X)
FFT Scaling Factor Ch5	0x3C8	8	FFT Mag. = RAM Data * 2 ^ (-X)
FFT Scaling Factor Ch6	0x3C9	8	FFT Mag. = RAM Data * 2 ^ (-X)
FFT Scaling Factor Ch7	0x3CA	8	FFT Mag. = RAM Data * 2 ^ (-X)
FFT Scaling Factor Ch8	0x3CB	8	FFT Mag. = RAM Data * 2 ^ (-X)
Gate Size	0x21C	16	Length of the "Gate" input. Unit: clock cycles.

Note: the following registers are not commonly used and do not need to be touched unless a specific configuration is required.

VME Interface Registers			
Register	Add.	Data Width	Description
Channel Mask	0x00	8	Bits <7:0> - Set masks for Ch8 to Ch1 respectively. Bit <7> for Ch8, Bit <0> for Ch1. "1" = ON, "0" = OFF. Example: "00000001" means only Ch1 active.
DCDC Mode	0x01	8	Bits <1,0> - "00" – Fixed frequency, "01" – sweep 10% frequency, "1X" – spread spectrum. Default = "00".
VME IRQ Interrupt Level	0x02	8	Bits <2:0> - Hex number indicates the VME IRQ line. "000" = No interrupt "001" = IRQ1, "002" = IRQ2, ...
VME A32 Pointer for ADC Raw Data	0x04	32	Indicates the starting address in memory for ADC raw data.
Channel Buffer Size for Raw Data	0x08	32	Indicates number of 32-bit words (two samples in each word) in memory reserved for each channel.
VME A24 Pointer for FPGA Flash Config. Data	0x24	32	
Buffer Size for FPGA Flash Config. Data	0x28	32	Indicates number of 32-bit words (two samples in each word) in memory reserved for each channel.
VME A24 Pointer for Digitizer Flash Settings Data	0x2C	32	
Buffer Size for Digitizer Flash Settings Data	0x30	32	Indicates number of 32-bit words (two samples in each word) in memory reserved for each channel.
VME A24 Pointer for	0x34	32	

Digitizer Flash Data			
Buffer Size for Digitizer Flash Data	0x38	32	Indicates number of 32-bit words (two samples in each word) in memory reserved for each channel.
Board ID (Read Only)	0x3C	32	Board ID, read only.
Generic Register 0	0x60	32	Available for software user.
Generic Register 1	0x64	32	Available for software user.
Generic Register 2	0x68	32	Available for software user.
Generic Register 3	0x6C	32	Available for software user.
Generic Register 4	0x70	32	Available for software user.
Generic Register 5	0x74	32	Available for software user.
Generic Register 6	0x78	32	Available for software user.
Generic Register 7	0x7C	32	Available for software user.

Interrupt			
Register	Add.	Data Width	Description
Software Set IRQ, #0 ~ #15	0x206	16	Bits <15:0> - IRQ15 ~ IRQ0. IRQ15 ~ IRQ12 not used in this design. Generate software interrupts by writing into register. Read back to see non-masked active interrupts (software or hardware generated).
VME IRQ Mask	0x290	16	Bits <11:0> - Mask for IRQ11 ~ IRQ0. "1" = Active, "0" = Disabled
IRQ Vector for IRQ #0	0x220	16	Active when ADC data out of range (any channel).
IRQ Vector for IRQ #1	0x222	16	Active at end of WB Gate #0
IRQ Vector for IRQ #2	0x224	16	Active at end of WB Gate #1
IRQ Vector for IRQ #3	0x226	16	Active at end of WB Gate #2
IRQ Vector for IRQ #4	0x228	16	Active at end of WB Gate #3
IRQ Vector for IRQ #5	0x22A	16	Active at end of WB Gate #4
IRQ Vector for IRQ #6	0x22C	16	Active at end of WB Gate #5
IRQ Vector for IRQ #7	0x22E	16	Active at end of WB Gate #6
IRQ Vector for IRQ #8	0x230	16	Active at end of WB Gate #7
IRQ Vector for IRQ #9	0x232	16	Active at end of NB Gate
IRQ Vector for IRQ #10	0x234	16	Active at start of digitizer mode
IRQ Vector for IRQ #11	0x236	16	Active at end of digitizer mode

SYNC Module Control Registers			
Register	Add.	Data Width	Description
Time Stamp Counter, Sync with TCLK Events	0x100	16	Bits <15:0> - Read back of time stamp counter. (Read Only)
TCLK Start Delay	0x102	16	Bits <15:0> - TCLK Start Delay.
TCLK Stop Delay	0x104	16	Bits <15:0> - TCLK Stop Delay.
TCLK Delay Scale	0x106	16	Bits <15:0> - TCLK Delay Scale.

BSYNC Start Delay	0x108	16	Bits <15:0> - BSYNC Start Delay.
BSYINC Stop Delay	0x10A	16	Bits <15:0> - BSYINC Stop Delay.
BSYNC Delay Scale	0x10C	16	Bits <15:0> - BSYNC Delay Scale.
TCLK Start Event	0x10E	8	Bits <7:0> - TCLK Start Event.
TCLK Stop Event	0x10F	8	Bits <7:0> - TCLK Stop Event.
BSYNC Start Event	0x110	8	Bits <7:0> - BSYNC Start Event.
BSYNC Stop Event	0x111	8	Bits <7:0> - BSYNC Stop Event.
SYNC In Source Mode	0x112	8	Bits <7:0> - Source for SYNC In signal on ATF. "0x0" = External Sync Signal, "0x1" = TCLK Start Event, "0x2" = TCLK Stop Event, "0x3" = BSYNC Start Event, "0x4" = BSYNC Stop Event.
Trigger Source Mode	0x113	8	Bits <7:0> - Source for Trigger signal on ATF. "0x0" = External Trigger Signal, "0x1" = TCLK Start Event, "0x2" = TCLK Stop Event, "0x3" = BSYNC Start Event, "0x4" = BSYNC Stop Event.
Gate Source Mode	0x114	8	Bits <7:0> - Source for Gate signal on ATF. "0x0" = External Gate Signal, "0x1" = TCLK Start/Stop Event, "0x2" = BSYNC Start/Stop Event.
SYNC Out Source Mode	0x115	8	Bits <7:0> - Source for Sync Out port. "0x0" = External Sync In, "0x1" = External Trigger, "0x2" = External Gate, "0x3" = TCLK Start Event, "0x4" = TCLK Stop Event, "0x5" = BSYNC Start Event, "0x6" = BSYNC Stop Event, "0x7" = ADC samples, "0x8" = Mode Active, "0x9" = ADC's clock, "0xA" = ATF-NB gate, "0xB" = ATF-WB gates, "0xC" = TBT gate, "0xD" = Turn Marker.

Sync IRQ

Register	Add.	Data Width	Description
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SYNC IRQ Mask	0x118	16	Bits <8:0> - Mask for SYNC IRQ8 ~ IRQ0. "1" = Active, "0" = Disabled
Software Set SYNC IRQ #0 ~ IRQ #15	0x11A	16	Bits <15:0> - SYNC IRQ15 ~ IRQ0. IRQ15 ~ IRQ9 not used in this design. Generate software interrupts by writing into register. Read back to see non-masked active interrupts (software or hardware generated).
IRQ Vector for IRQ #0	0x120	16	Active on external Sync Signal.
IRQ Vector for IRQ #1	0x122	16	Active on external Trigger signal.
IRQ Vector for IRQ #2	0x124	16	Active on external Gate signal positive edge.
IRQ Vector for IRQ #3	0x126	16	Active on external Gate signal negative edge.
IRQ Vector for IRQ #4	0x128	16	Active on TCLK Start event.
IRQ Vector for IRQ #5	0x12A	16	Active on TCLK Stop event.
IRQ Vector for IRQ #6	0x12C	16	Active on BSYNC Start event.
IRQ Vector for IRQ #7	0x12E	16	Active on BSYNC Stop event.
IRQ Vector for IRQ #8	0x130	16	Active on TCLK time stamp counter reset.

ADC Chip 1 ADS6445 Registers (All registers are 11 bits – D16)			
Register	Addr.	Default	Description
Power Down Modes Reg. A	0x80	0x00	Bits <9:6> - Not Used. Must be "0". Bit <10> - Software Reset. "1" resets all internal registers and self-clears to "0". Bit <5> - Reference. "0"=Internal Reference Enabled, "1"=External Reference Enabled. Bits <4:1> - Channels 4~1 Power Down. "1"=Power Down, "0"=Normal Operation. Bit <0> - Global Power Down, including channels 1~4. "1"=Power Down, "0"=Normal Operation.
Input Clock Gain Reg. B	0x82	0x00	Bits <10:7, 1:0> - Not Used. Must be "0". Bits <6:2> - CLKIN Gain. "11000" Gain 0, minimum gain "00000" Gain 1, default gain after reset "01100" Gain 2 "01010" Gain 3 "01001" Gain 4 "01000" Gain 5, maximum gain
Capture Test Pattern Reg. C	0x84	0x200	Bits <10, 8, 4:0> - Not Used. Must be "0". Bit <9> - Data Format Selection. "0" = 2's Complement format "1" = Straight binary format Bits <7:5> - Capture Test Patterns. 000 Normal ADC operation 001 Output all zeros 010 Output all ones 011 Output toggle pattern

			<p>100 Unused</p> <p>101 Output custom pattern (contents of CUSTOM pattern registers 0x86 and 0x88)</p> <p>110 Output DESKEW pattern (serial stream of 1010...)</p> <p>111 Output SYNC pattern</p>
Test Patterns Reg. D	0x86	0xAA	<p>Bits <10:0> - Lower 11 bits of custom pattern. D10 D9 D8 ... D0</p>
Fine Gain Reg. E	0x88	0x02	<p>Bits <2:0> - Upper 3 bits of custom pattern. D13 D12 D11</p> <p>Bits <7:3> - Not Used. Must be "0".</p> <p>Bits <10:8> - Fine Gain Control.</p> <p>000 0dB Gain (full-scale range=2.00VPP)</p> <p>001 1dB Gain (full-scale range=1.78VPP)</p> <p>010 2dB Gain (full-scale range=1.59VPP)</p> <p>011 3dB Gain (full-scale range=1.42VPP)</p> <p>100 4dB Gain (full-scale range=1.26VPP)</p> <p>101 5dB Gain (full-scale range=1.12VPP)</p> <p>110 6dB Gain (full-scale range=1.00VPP)</p>
Output Data Config. Reg. F	0x8A	0x00	<p>Bit <10> - Over-Ride Bit. All the functions in this register can also be controlled using the parallel control pins. By setting this bit to "1", the contents of register will over-ride the settings of the parallel pins.</p> <p>Bits <9:8, 3> - Not Used. Must be "0".</p> <p>Bit <7> - Byte/bit Wise outputs. "0": Byte wise, "1": bit wise.</p> <p>Bit <6> - MSB or LSB First Selection. "0": MSB First, "1": LSB First.</p> <p>Bit <5> - Coarse Gain Control. "0"=0dB Coarse Gain (full-scale range=2.0 VPP), "1"=3.5dB Coarse Gain (full-scale range=1.34 VPP)</p> <p>Bit <4> - Bit Clock Capture Edge (only when SDR bit clock is selected, Bit 1 = "1"). "0"=Capture data with falling edge of bit clock, "1"=Capture data with rising edge of bit clock.</p> <p>Bit <2> - Serialization Factor Selection. "0"=14x Serialization, "1"=16x Serialization.</p> <p>Bit <1> - Bit Clock Selection (only in 2-wire interface). "0"=DDR Bit Clock, "1"=SDR Bit Clock.</p> <p>Bit <0> - Interface Selection. "0"=1 Wire interface, "1"=2 Wire interface.</p>
Data Interface Reg. G	0x8C	0x140	<p>Bit <0> - LVDS Current Double For Data Outputs. "0"=Nominal LVDS current, as set by Bits <5:2>. "1"=Double the nominal value.</p> <p>Bit <1> - LVDS Current Double for Bit and Word Clock Outputs. "0"=Nominal LVDS current, as set by Bits<5:2>. "1"=Double the nominal value.</p>

			<p>Bits <3:2> - LVDS Current Setting for Data Outputs.</p> <p>00 3.5mA 01 4mA 10 2.5mA 11 3mA</p> <p>Bits <5:4> - CVDS Current Setting For Bit and Word Clock Outputs.</p> <p>00 3.5mA 01 4mA 10 2.5mA 11 3mA</p> <p>Bits <10:6> - LVDS Internal Termination For Bit and Word Clock outputs.</p> <p>“00000” No internal termination “00001” 166 Ω “00010” 200 Ω “00100” 250 Ω “01000” 333 Ω “10000” 500 Ω</p> <p>Any combination of above bits can be programmed, resulting in a parallel combination of the selected values. For example, “00101” is the parallel combination of 166 250=100 Ω “00101” 100 Ω</p>
Data Interface Reg. H	0x8E	0x05	<p>Bits <10:9> - Only when 2-wire interface is selected.</p> <p>“00” Byte-wise or bitwise output, 1x frame clock “11” Word-wise output enabled, 0.5x frame clock</p> <p>Bits <8:5> - Not Used. Must be “0”.</p> <p>Bits <4:0> - LVDS Internal Termination For Data Outputs.</p> <p>“00000” No internal termination “00001” 166 Ω “00010” 200 Ω “00100” 250 Ω “01000” 333 Ω “10000” 500 Ω</p> <p>Any combination of above bits can be programmed, resulting in a parallel combination of the selected values. For example, “00101” is the parallel combination of 166 250=100 Ω “00101” 100 Ω</p>

ADC Chip 2 ADS6445 Registers (All registers are 11 bits – D16)

Register	Addr.	Default	Description
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Power Down Modes Reg. A	0x90	0x00	<p>Bits <9:6> - Not Used. Must be "0".</p> <p>Bit <10> - Software Reset. "1" resets all internal registers and self-clears to "0".</p> <p>Bit <5> - Reference. "0"=Internal Reference Enabled, "1"=External Reference Enabled.</p> <p>Bits <4:1> - Channels 8~5 Power Down. "1"=Power Down, "0"=Normal Operation.</p> <p>Bit <0> - Global Power Down, including channels 5~8. "1"=Power Down, "0"=Normal Operation.</p>
Input Clock Gain Reg. B	0x92	0x00	<p>Bits <10:7, 1:0> - Not Used. Must be "0".</p> <p>Bits <6:2> - CLKIN Gain.</p> <p>"11000" Gain 0, minimum gain</p> <p>"00000" Gain 1, default gain after reset</p> <p>"01100" Gain 2</p> <p>"01010" Gain 3</p> <p>"01001" Gain 4</p> <p>"01000" Gain 5, maximum gain</p>
Capture Test Pattern Reg. C	0x94	0x200	<p>Bits <10, 8, 4:0> - Not Used. Must be "0".</p> <p>Bit <9> - Data Format Selection.</p> <p>"0" = 2's Complement format</p> <p>"1" = Straight binary format</p> <p>ts <7:5> - Capture Test Patterns.</p> <p>000 Normal ADC operation</p> <p>001 Output all zeros</p> <p>010 Output all ones</p> <p>011 Output toggle pattern</p> <p>100 Unused</p> <p>101 Output custom pattern (contents of CUSTOM pattern registers 0x86 and 0x88)</p> <p>110 Output DESKEW pattern (serial stream of 1010...)</p> <p>111 Output SYNC pattern</p>
Test Patterns Reg. D	0x96	0xAA	<p>Bits <10:0> - Lower 11 bits of custom pattern.</p> <p>D10 D9 D8 ... D0</p>
Fine Gain Reg. E	0x98	0x02	<p>Bits <2:0> - Upper 3 bits of custom pattern.</p> <p>D13 D12 D11</p> <p>Bits <7:3> - Not Used. Must be "0".</p> <p>Bits <10:8> - Fine Gain Control.</p> <p>000 0dB Gain (full-scale range=2.00VPP)</p> <p>001 1dB Gain (full-scale range=1.78VPP)</p> <p>010 2dB Gain (full-scale range=1.59VPP)</p> <p>011 3dB Gain (full-scale range=1.42VPP)</p> <p>100 4dB Gain (full-scale range=1.26VPP)</p> <p>101 5dB Gain (full-scale range=1.12VPP)</p> <p>110 6dB Gain (full-scale range=1.00VPP)</p>
Output Data Config. Reg. F	0x9A	0x00	<p>Bit <10> - Over-Ride Bit. All the functions in this register can also be controlled using the parallel control pins. By setting this bit to "1", the contents of</p>

			<p>register will over-ride the settings of the parallel pins. Bits <9:8, 3> - Not Used. Must be "0". Bit <7> - Byte/bit Wise outputs. "0": Byte wise, "1": bit wise. Bit <6> - MSB or LSB First Selection. "0": MSB First, "1": LSB First. Bit <5> - Coarse Gain Control. "0"=0dB Coarse Gain (full-scale range=2.0 VPP), "1"=3.5dB Coarse Gain (full-scale range=1.34 VPP) Bit <4> - Bit Clock Capture Edge (only when SDR bit clock is selected, Bit 1 = "1"). "0"=Capture data with falling edge of bit clock, "1"=Capture data with rising edge of bit clock. Bit <2> - Serialization Factor Selection. "0"=14x Serialization, "1"=16x Serialization. Bit <1> - Bit Clock Selection (only in 2-wire interface). "0"=DDR Bit Clock, "1"=SDR Bit Clock. Bit <0> - Interface Selection. "0"=1 Wire interface, "1"=2 Wire interface.</p>
Data Interface Reg. G	0x9C	0x140	<p>Bit <0> - LVDS Current Double For Data Outputs. "0"=Nominal LVDS current, as set by Bits <5:2>. "1"=Double the nominal value. Bit <1> - LVDS Current Double for Bit and Word Clock Outputs. "0"=Nominal LVDS current, as set by Bits<5:2>. "1"=Double the nominal value. Bits <3:2> - LVDS Current Setting for Data Outputs. 00 3.5mA 01 4mA 10 2.5mA 11 3mA Bits <5:4> - CVDS Current Setting For Bit and Word Clock Outputs. 00 3.5mA 01 4mA 10 2.5mA 11 3mA Bits <10:6> - LVDS Internal Termination For Bit and Word Clock outputs. "00000" No internal termination "00001" 166 Ω "00010" 200 Ω "00100" 250 Ω "01000" 333 Ω "10000" 500 Ω Any combination of above bits can be programmed, resulting in a parallel combination of the selected values. For example, "00101" is the parallel</p>

			combination of 166 250=100 Ω "00101" 100 Ω
Data Interface Reg. H	0x9E	0x05	<p>Bits <10:9> - Only when 2-wire interface is selected. "00" Byte-wise or bitwise output, 1x frame clock "11" Word-wise output enabled, 0.5x frame clock Bits <8:5> - Not Used. Must be "0". Bits <4:0> - LVDS Internal Termination For Data Outputs. "00000" No internal termination "00001" 166 Ω "00010" 200 Ω "00100" 250 Ω "01000" 333 Ω "10000" 500 Ω</p> <p>Any combination of above bits can be programmed, resulting in a parallel combination of the selected values. For example, "00101" is the parallel combination of 166 250=100 Ω "00101" 100 Ω</p>

ADC Overflow			
Register	Add.	Data Width	Description
ADC's OVR Status	0x2AD	8	Bits <7:0> - Denotes ADC data saturation for channels 8 to 1. Example: Bit <7> = Ch8. "1" = Overflow, "0" = Normal.
ADC 1 Abs Max Count	0x370	16	ADC data max count recorder for channel 1.
ADC 2 Abs Max Count	0x372	16	ADC data max count recorder for channel 2.
ADC 3 Abs Max Count	0x374	16	ADC data max count recorder for channel 3.
ADC 4 Abs Max Count	0x376	16	ADC data max count recorder for channel 4.
ADC 5 Abs Max Count	0x378	16	ADC data max count recorder for channel 5.
ADC 6 Abs Max Count	0x37A	16	ADC data max count recorder for channel 6.
ADC 7 Abs Max Count	0x37C	16	ADC data max count recorder for channel 7.
ADC 8 Abs Max Count	0x37E	16	ADC data max count recorder for channel 8.

ADC Delays			
Register	Add.	Data Width	Description
ADC 1 Data Delay	0x140	8	Bits <4:0> - Data delay for channel 1, in ADC samples. Ranges from "0" to "31". Default is 16.
ADC 2 Data Delay	0x141	8	Bits <4:0> - Data delay for channel 2, in ADC samples. Ranges from "0" to "31". Default is 16.
ADC 3 Data Delay	0x142	8	Bits <4:0> - Data delay for channel 3, in ADC samples. Ranges from "0" to "31". Default is 16.
ADC 4 Data Delay	0x143	8	Bits <4:0> - Data delay for channel 4, in ADC

			samples. Ranges from "0" to "31". Default is 16.
ADC 5 Data Delay	0x144	8	Bits <4:0> - Data delay for channel 5, in ADC samples. Ranges from "0" to "31". Default is 16.
ADC 6 Data Delay	0x145	8	Bits <4:0> - Data delay for channel 6, in ADC samples. Ranges from "0" to "31". Default is 16.
ADC 7 Data Delay	0x146	8	Bits <4:0> - Data delay for channel 7, in ADC samples. Ranges from "0" to "31". Default is 16.
ADC 8 Data Delay	0x147	8	Bits <4:0> - Data delay for channel 8, in ADC samples. Ranges from "0" to "31". Default is 16.

Clock Driver			
Register	Addr.	Data Width	Description
Control Register 0 (Output Divider 0)	0xA0	32	<p>Bits <0:1> - Pre-Divider selection for primary reference. "00" = 3-state, "01" = divide by 1, "10", divide by 2, "11" = reserved.</p> <p>Bits <4:5> - Output Mux 0 Select. "00" = PRI_IN (On board oscillator), "01" = SEC_IN (External clock), "10" = SMART_MUX, "11" = VCO_CORE.</p> <p>Bits <12:6> - Coarse phase adjust select for output 0.</p> <p>Bits <19:13> - Output Divider 0 Ratio Select. Bit <20> - "1" = output 0 enabled, "0" = disabled.</p> <p>Bit <21> - High swing LVPEC when set to "1", normal swing when set to "0". Bits <3:2> - Reserved. Bits <26:27> - Output buffer select 0.</p> <p>Bits <22:23> - LVCMOS mode select for Output 0 positive pin. "00" = Active, "10" = Inverting, "11" = Low, "01" = 3-state.</p> <p>Bits <24:25> - LVCMOS mode select for Output 0 negative pin. "00" = Active, "10" = Inverting, "11" = Low, "01" = 3-state.</p>
Control Register 1 (Output Divider 1)	0xA4	32	<p>Bits <0:1> - Pre-Divider selection for secondary reference. "00" = 3-state, "01" = divide by 1, "10", divide by 2, "11" = reserved.</p> <p>Bits <4:5> - Output Mux 1 Select. "00" = PRI_IN (On board oscillator), "01" = SEC_IN (External clock), "10" = SMART_MUX, "11" = VCO_CORE.</p> <p>Bits <12:6> - Coarse phase adjust select for output 1.</p> <p>Bits <19:13> - Output Divider 1 Ratio Select. Bit <20> - "1" = output 1 enabled, "0" = disabled.</p> <p>Bit <21> - High swing LVPEC when set to "1", normal swing when set to "0". Bits <3:2> - Reserved. Bits <26:27> - Output buffer select 1.</p> <p>Bits <22:23> - LVCMOS mode select for Output 1</p>

			<p>positive pin. "00" = Active, "10" = Inverting, "11" = Low, "01" = 3-state.</p> <p>Bits <24:25> - LVCMOS mode select for Output 1 negative pin. "00" = Active, "10" = Inverting, "11" = Low, "01" = 3-state.</p>
Control Register 2 (Output Divider 2)	0xA8	32	<p>Bit<0> - Reference divider bit 0. Bit<1> - Reference divider bit 1. Bits <3:2> - Reserved. Bits <26:27> - Output buffer select 2.</p> <p>Bits <4:5> - Output Mux 2 Select. "00" = PRI_IN (On board oscillator), "01" = SEC_IN (External clock), "10" = SMART_MUX, "11" = VCO_CORE.</p> <p>Bits <12:6> - Coarse phase adjust select for output 2.</p> <p>Bits <19:13> - Output Divider 2 Ratio Select. Bit <20> - "1" = output 2 enabled, "0" = disabled.</p> <p>Bit <21> - High swing LVPEEC when set to "1", normal swing when set to "0".</p> <p>Bits <22:23> - LVCMOS mode select for Output 2 positive pin. "00" = Active, "10" = Inverting, "11" = Low, "01" = 3-state.</p> <p>Bits <24:25> - LVCMOS mode select for Output 2 negative pin. "00" = Active, "10" = Inverting, "11" = Low, "01" = 3-state.</p>
Control Register 3 (Output Divider 3)	0xAC	32	<p>Bit<0> - Reference divider bit 2. Bits <3:1> - Reserved. Bits <26:27> - Output buffer select 3.</p> <p>Bits <4:5> - Output Mux 3 Select. "00" = PRI_IN (On board oscillator), "01" = SEC_IN (External clock), "10" = SMART_MUX, "11" = VCO_CORE.</p> <p>Bits <12:6> - Coarse phase adjust select for output 3.</p> <p>Bits <19:13> - Output Divider 3 Ratio Select. Bit <20> - "1" = output 3 enabled, "0" = disabled.</p> <p>Bit <21> - High swing LVPEEC when set to "1", normal swing when set to "0".</p> <p>Bits <22:23> - LVCMOS mode select for Output 3 positive pin. "00" = Active, "10" = Inverting, "11" = Low, "01" = 3-state.</p> <p>Bits <24:25> - LVCMOS mode select for Output 3 negative pin. "00" = Active, "10" = Inverting, "11" = Low, "01" = 3-state.</p>
Control Register 4 (Output Divider 4)	0xB0	32	<p>Bit<0> - Reserved, must be set to "1". Bits <3:1> - Reserved.</p> <p>Bits <4:5> - Output Mux 4 Select. "00" = PRI_IN (On board oscillator), "01" = SEC_IN (External clock), "10" = SMART_MUX, "11" = VCO_CORE.</p> <p>Bits <12:6> - Coarse phase adjust select for output 4.</p> <p>Bits <19:13> - Output Divider 4 Ratio Select. Bit <20> - "1" = output 4 enabled, "0" = disabled.</p> <p>Bit <21> - High swing LVPEEC when set to "1", normal</p>

			<p>swing when set to "0". Bits <26:27> - Output buffer select 4.</p> <p>Bits <22:23> - LVCMOS mode select for Output 4 positive pin. "00" = Active, "10" = Inverting, "11" = Low, "01" = 3-state.</p> <p>Bits <24:25> - LVCMOS mode select for Output 4 negative pin. "00" = Active, "10" = Inverting, "11" = Low, "01" = 3-state.</p>
Control Register 5	0xB4	32	<p>Bits <0:1> - Input buffer select. "01" = LVPECL, "11" = LVDS, "00" = LVCMOS. Bits <2:4> - EEPROM clock select. Bit <5> - EEPROM clock select enable.</p> <p>Bit <6> - Input buffer termination. "1" = DC, "0" = AC. Bit <7> - Input buffers hysteresis enable, "1" recommended.</p> <p>Bit <8> - Primary input termination. "0" = enable, "1" = disable. Bit <9> - Primary input negative pin biased with internal Vbb voltage when set to "1".</p> <p>Bit <10> - Secondary input negative pin biased with internal Vbb voltage when set to "1". Bits <13:12> - Reserved, must be "0".</p> <p>Bit <11> - Fail Safe is enabled for all input buffers when set to "1", DC coupling only. Bits <21:14> - Input Divider settings.</p> <p>Bits <25:22> - Lock-detect window width. "0000" = Narrow window, "0001", "0010", "0100", "0101", ... "1110" = Widest window, "XX11" = Reserved.</p> <p>Bit <26> - "0" = triggers after first lock detection, "1" = triggers after 64 cycles of lock detection.</p> <p>Bit <27> - "0" selects digital PLL Lock 0, "1" selects digital PLL Lock 1.</p>
Control Register 6	0xB8	32	<p>Bit <0> - VCO select, "0": VCO1 (low range), "1": VCO2 (high range). Bits <2:1> - Pre-scaler setting.</p> <p>Bits <23, 11> - Reserved, must be set to "0".</p> <p>Bits <15:13> - Bypass Divider setting. Bits <10:3> - Feedback Divider setting. Bit <26> - "1" = External loop filter is used, "0" = Internal loop filter is used.</p> <p>Bit <12> - "0" = Secondary input buffer internal termination enabled, "1" = Secondary internal termination circuitry disabled.</p> <p>Bit <20> - "0" = outputs synchronized to reference input on low-to-high pulse on SYNC pin, "1" = outputs synchronized to SYNC high-to-low pulse.</p> <p>Bit <21> - "1" = Wide pulse, "0" = Narrow pulse. Bit <22> - Enable VCO calibration command. Bit <24> - Enable auxiliary output when set to "1".</p> <p>Bit <25> - Select the output that will drive AUX output. "0" = Output divider 2, "1" = divider 3.</p>

			Bit <27> - "1": Calibration mode = Manual mode, "0": Calibration mode = startup mode. Bits <19:16> - Charge Pump current select.
Control Register 7	0xBC	32	Bits <20:0> - Loop filter control setting. Bit <21> - Reserved, must be set to "0". Bits <24, 22> - Diagnostics, set to "1". Bits <25, 23> - Smart Mux. "0" enables short delay for fast operation, "1" for long delay. Bit <26> - Read only. "0" = EEPROM unlock. "1" = EEPROM locked. Bit <27> - Reserved, always reads "1".
Control Register 8	0xC0	32	Bits <5:0> - Calibration read back from device. Bit <6> - Read only, status of the PLL lock pin driven by the device. Bit <7> - "0" = Set device Sleep mode ON, "1" = Normal mode. Bit <8> - "0" = Forces /SYNC, "1" = exit Sync. Bits <20, 13, 9> - Reserved, must be set to "0". Bits <12:10> - Silicon Revision. Bits <24:21, 19:14> - Factor registers. Bits <27:24> - Synthesizer Source Indicator.
Unlock CDCE62005	0xC4	8	Write Only. Bit <0> - Unlock CDCE62005.
Lock CDCE62005	0xC5	8	Write Only. Bit <0> - Copy data from RAM to EEPROM. Use discouraged.
Oscillator Enable	0xC6	8	Bit <0> - "1" – Enable internal oscillator for ADC clock.
Clock Reference Select	0xC7	8	Bit <0> - By pin, optional to SPI
Clock Base SYNC	0xC8	8	Bit <0> - By pin, optional to SPI
Clock Base Power Down	0xC9	8	Bit <0> - By pin, optional to SPI
Clock Base PLL Lock	0xCA	8	Bit <0> - "1" – PLL locked.

Flash			
Register	Addr.	Data Width	Description
Write Enable	0x160	8	Write command to enable write ops to Flash.
Write Disable	0x161	8	Write command to disable write ops to Flash.
Read/Write Status	0x162	8	Read/Write to Flash status register.
Erase Bulk	0x163	8	Write command to erase bulk in Flash.
Read Flash Chip ID	0x164	8	Read Flash ID.
Erase Sector	0x168	32	Write command to erase sector of Flash. Bits <23:0> - Number of sectors.

Remote Update

Register	Address	Data Width	Description
Read Master State Machine (MSM) Current State Mode	0x180	8	NA
Read Past Status 1 MSM Mode	0x181	8	NA
Read Current Application Mode Watch Dog Enable	0x182	8	NA
Read Past Status 1 Reconfiguration Trigger Conditions Source	0x183	8	NA
Read Past Status 2 MSM Mode	0x184	8	NA
Read Past Status 2 Reconfiguration Trigger Conditions Source	0x185	8	NA
R/W the Early Conf_Done Check	0x186	8	NA
R/W Watchdog Enable Value	0x187	8	NA
R/W The Osc_Internal Option	0x188	8	NA
R/W Watchdog Timeout Value	0x18A	16	NA
Read Current Application Mode Watchdog Time Value	0x18C	32	NA
Read Past Status 1 Boot Address	0x190	32	NA
Read Past Status 2 Boot Address	0x194	32	NA
R/W Boot Address (Upper 22 bits of 24 bit address value)	0x198	32	NA
Read Current Factory Mode Boot Address 24 bit	0x19C	32	NA
Write the Command to Reconfigure FPGA	0x1A0	8	NA
Write the Command to Reset Watchdog Timer	0x1A6	8	NA

8. Connectors and Switches

