

# Digital Down Converter

**125 MHz Digitizer Firmware Description**

# Update Notes: Ver. FAD03

ver FAD02:

With settings and added features for switchyard BPMs.

ver FAD03:

Added coefficient reloading for two FIR filters.

Fixed Magnitude/Intensity real time data reporting interrupts.

ver FAD05:

Expanded down converter output mux. Fixed problems caused by it.

ver FAD08:

Using custom filter coefficients. Bug fixes.

# 125 MHz Digitizer

[ 6U VME Board

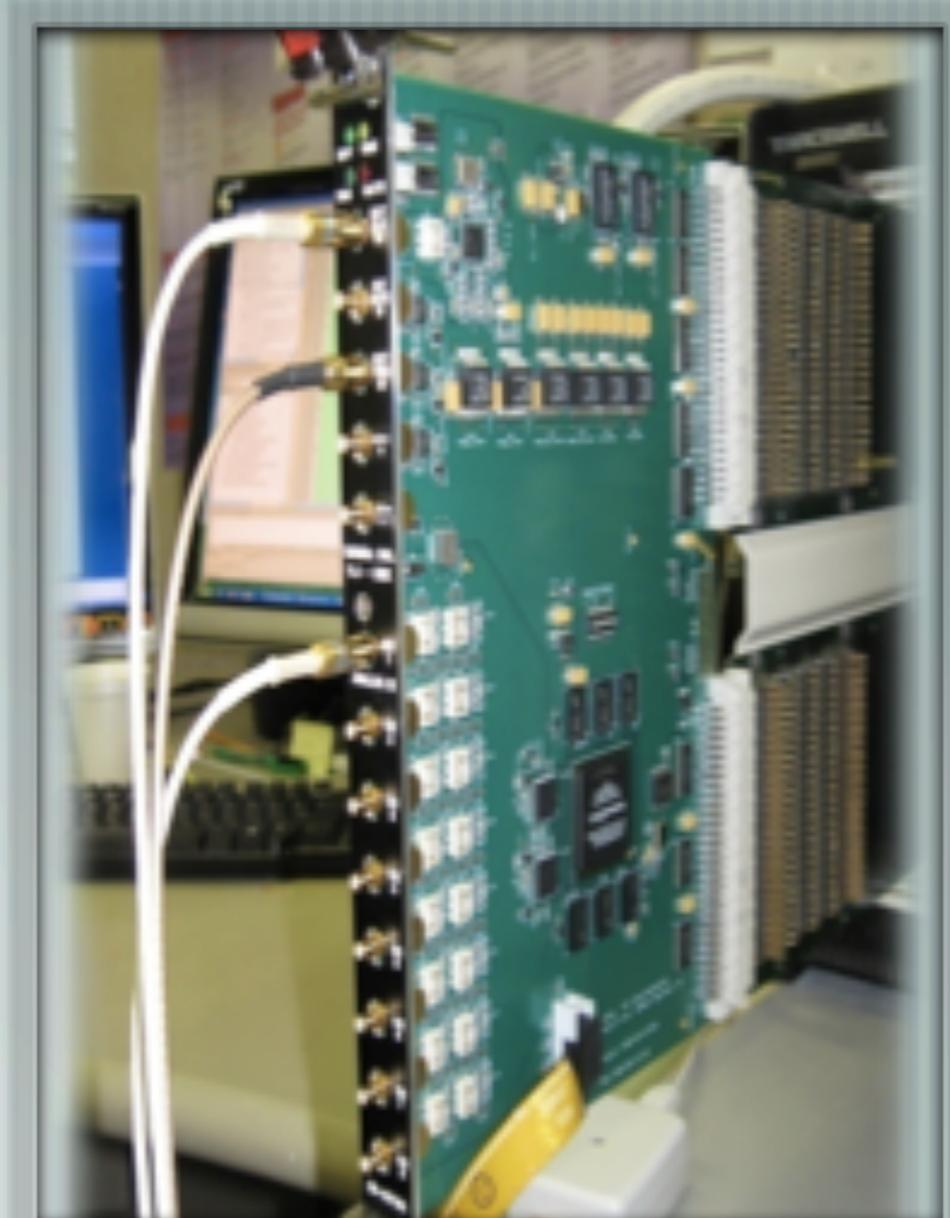
[ 8 channels, 14 bit ADC @ 125MSPS

[ Selectable AC/DC coupling

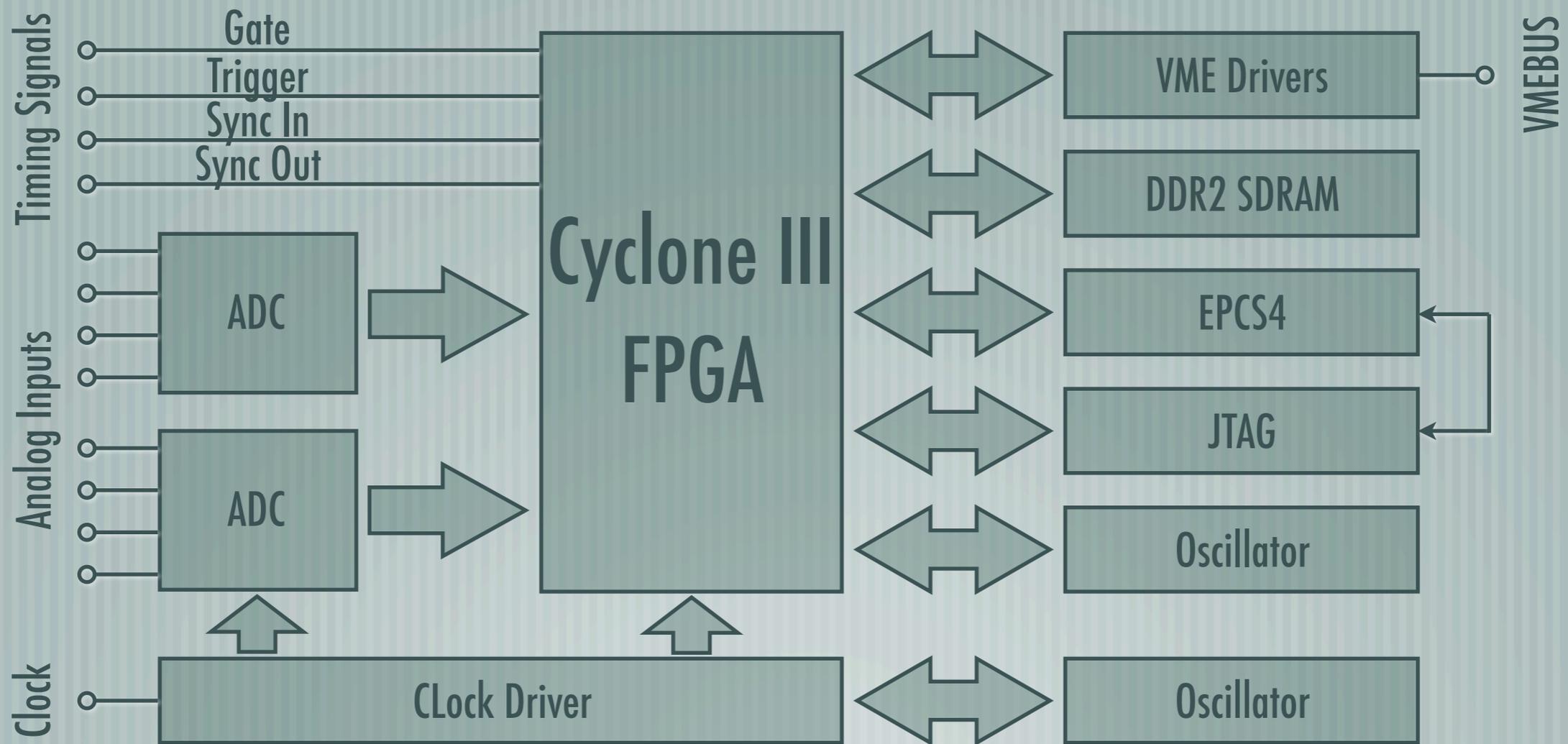
[ Hardware & software data processing

[ 16M samples per channel buffering

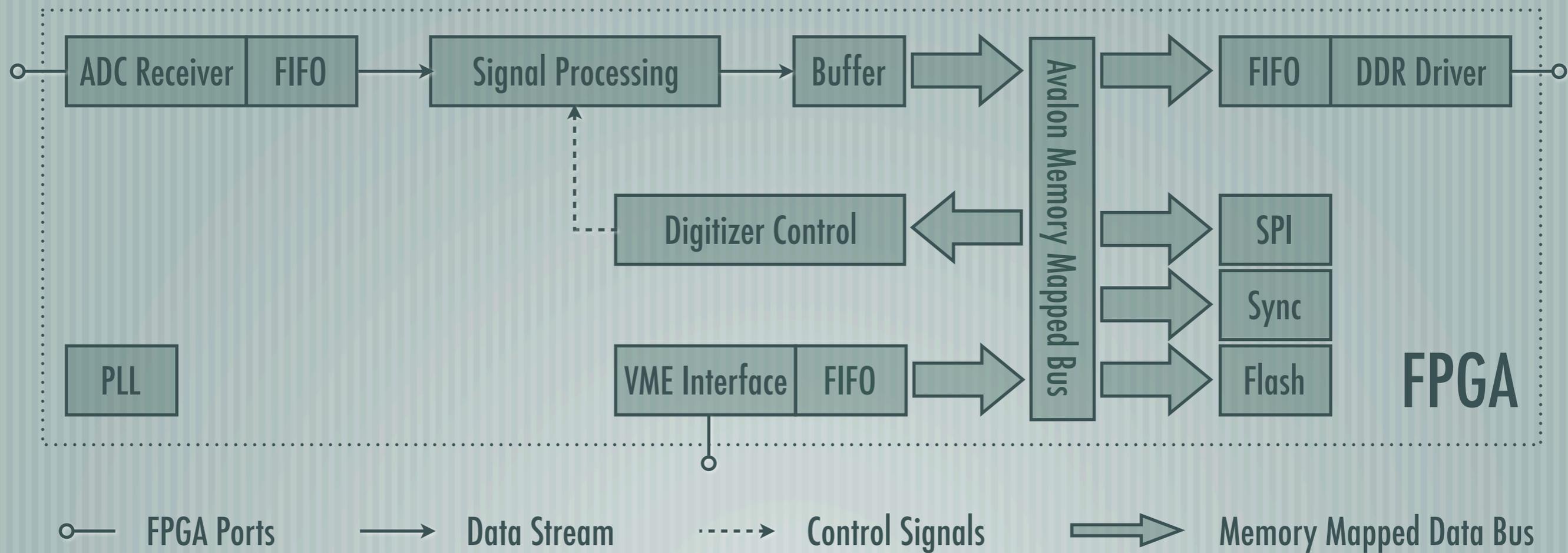
[ Smart triggering based on FPGA



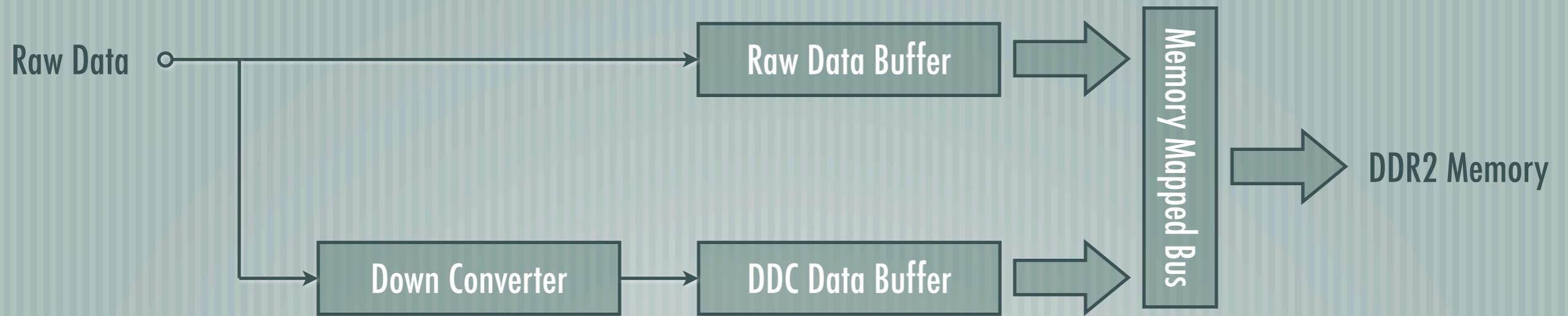
# Hardware Block Diagram



# Firmware Structure



# Data Paths

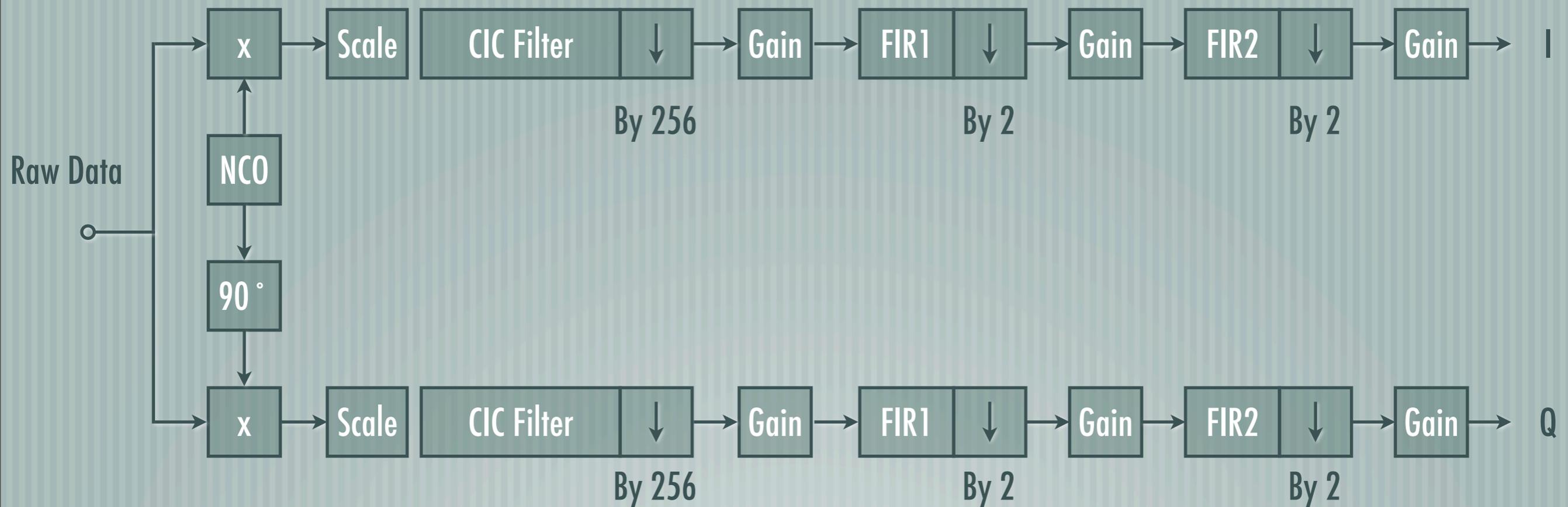


Each data path can be turned on or off through registers.

Number of data points saved from each data path is programmable through registers.

Raw data may be decimated to reduce data bus usage.

# Digital Down Converter

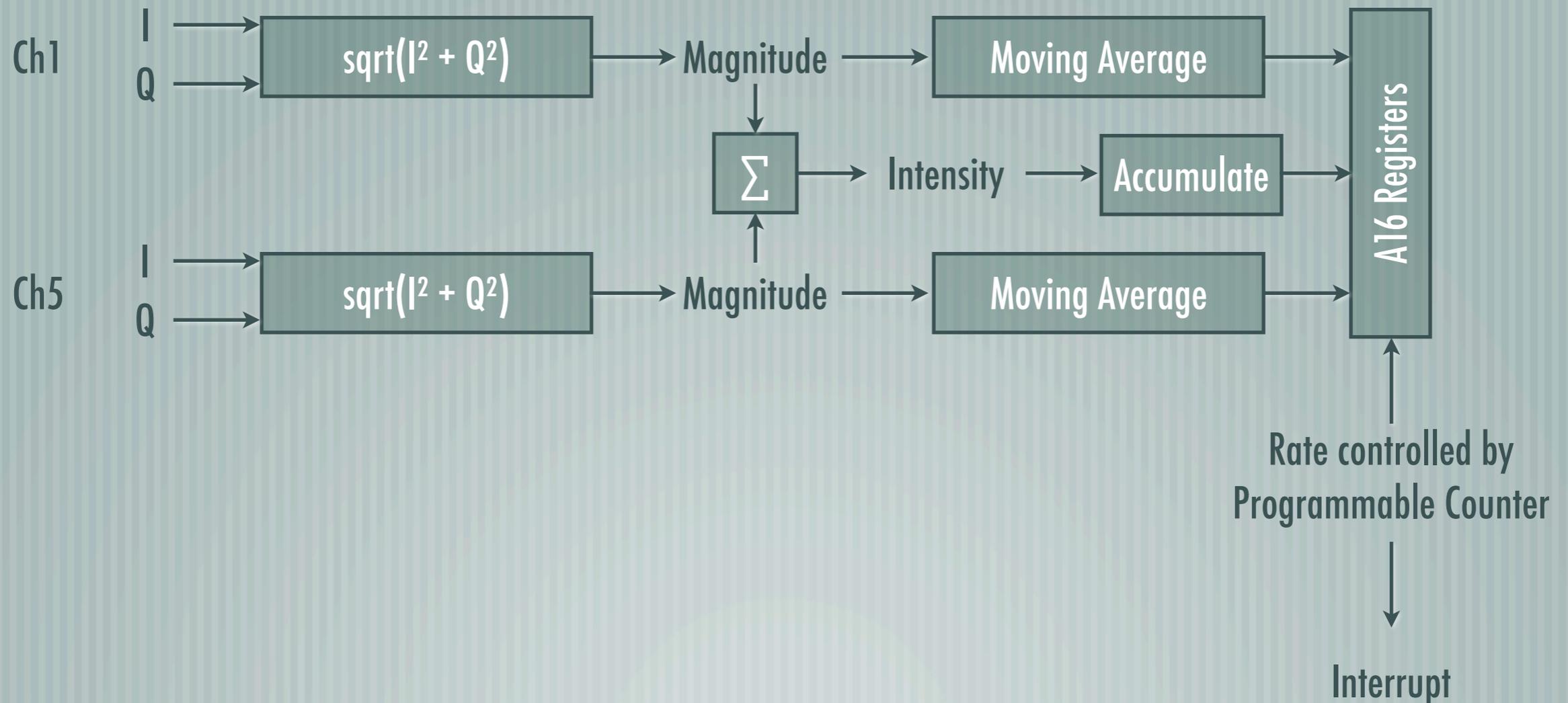


5-stage CIC filter, decimation rate is 256.

64-tap low pass FIR filters, decimation by 2.

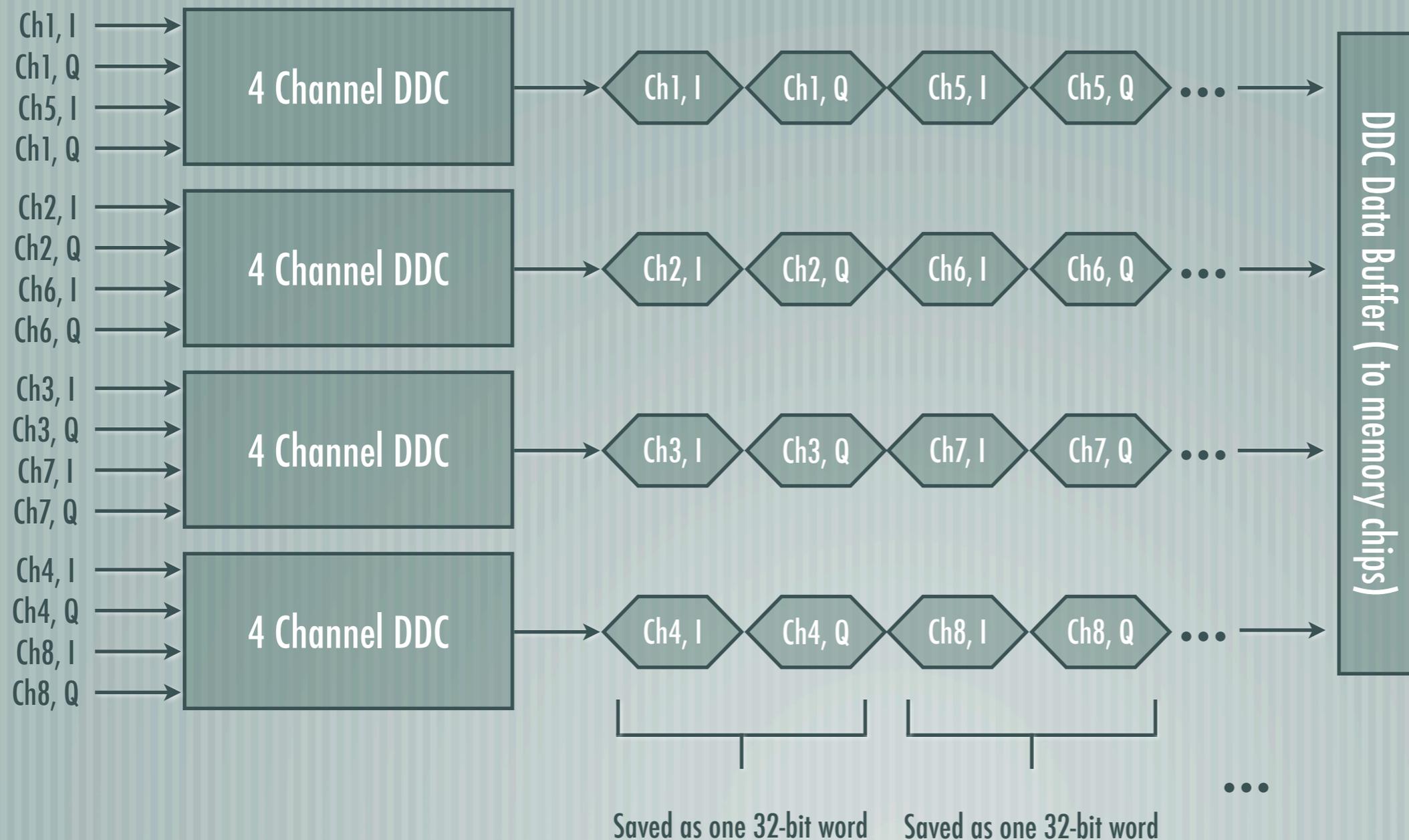
Scale and gain adjustment stages programmable through registers.

# Real time data reporting

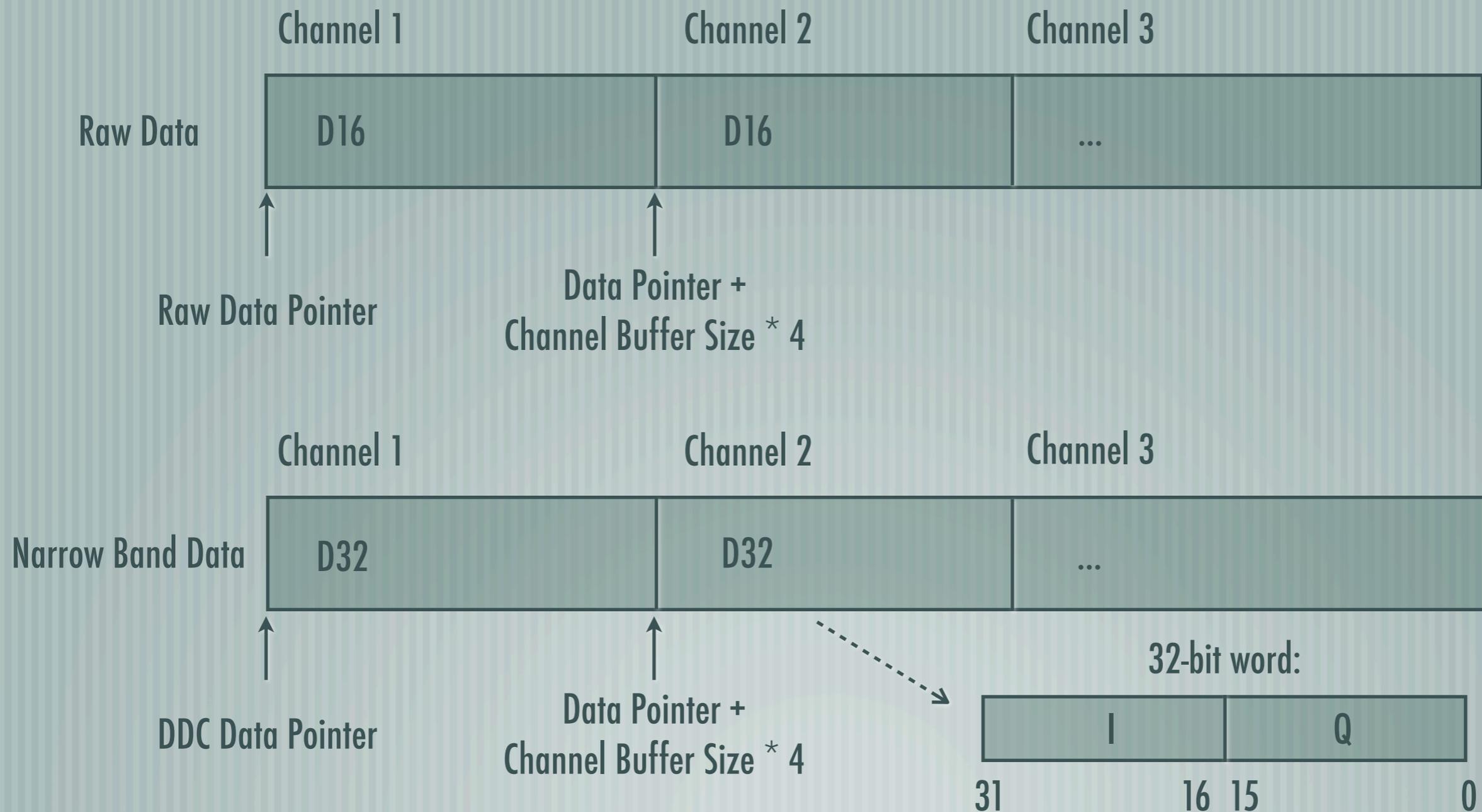


Channel 1 + Channel 5, Channel 2 + Channel 6, Channel 3 + Channel 7, Channel 4 + Channel 8

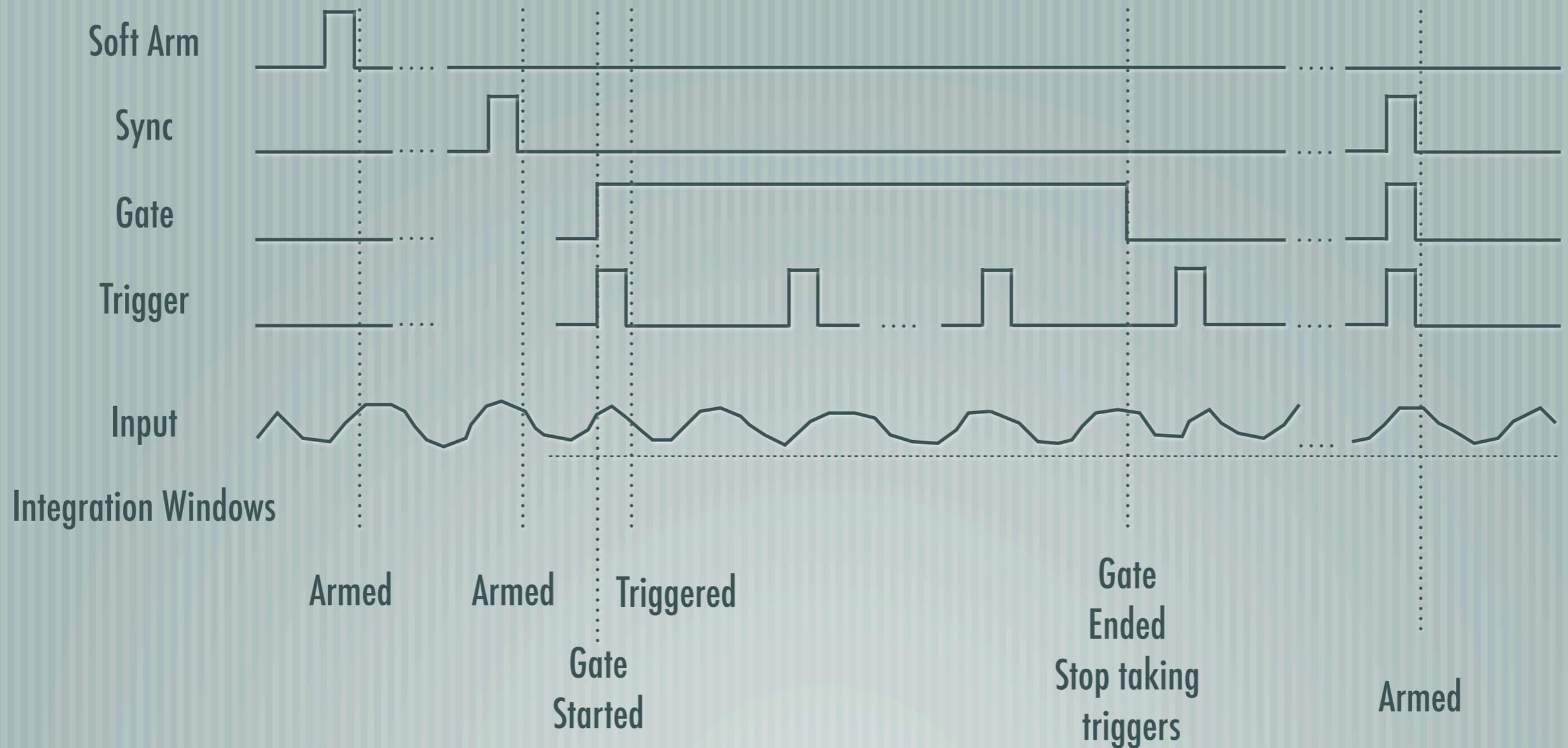
# A32 Data Multiplexing



# VME A32 Address Map



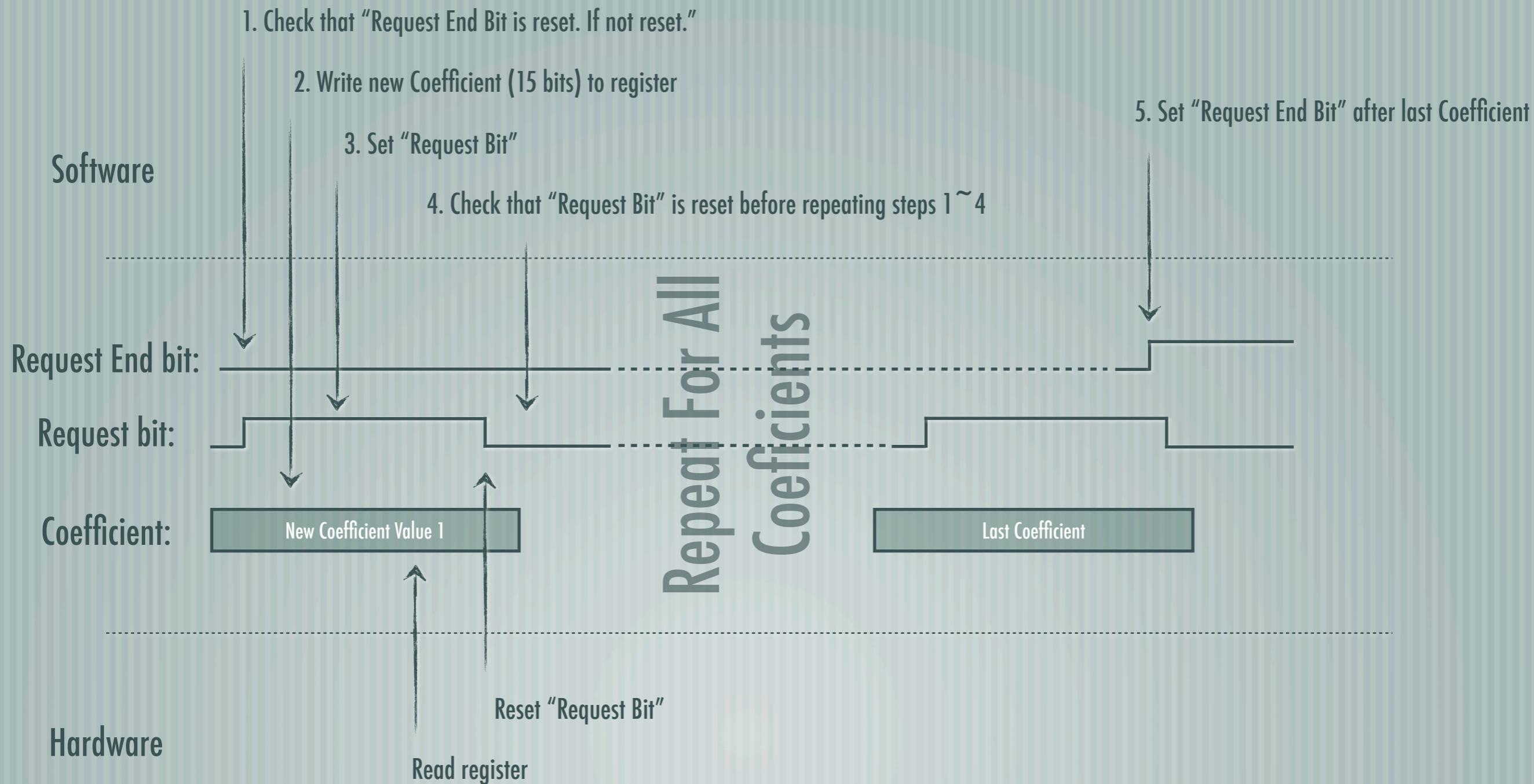
# Timing Diagram



ADC and Down Converter run constantly. Data saving only takes place when specified trigger conditions are met.

Sync (External arm), Gate and Trigger can be omitted in the diagram if not selected by the "Run Mode" register.

# FIR Coefficients Reloading



# Registers

— [ All registers are in A16 space.

— [ Data widths of registers are as noted.

— [ Registers are read/write unless described otherwise.

— [ For details on the ADC chips see data sheets of ADS6445.

— [ For details on the clock driver see CDCE62005.

— [ Default clock register values: clock rate =  $\sim 78.06$  .

# Registers: Default Values

Register	Address	Data Width	Default
Digitizer Mode	0x200	8	0x82
Number of Raw Samples	0x20C	32	0x2000
NCO Frequency	0x238	32	0x2100002B
CIC Decimation Rate	0x23C	16	0x1AC
CIC Gain	0x23E	8	0x2
FIR Gain	0x23F	8	0x1
DDC Number of Samples	0x240	32	0x2000
DDC Output Mux	0x298	8	0x3
A32 Pointer for Raw Data	0x04	32	0x08000000
Channel Buffer Size for Raw Data	0x08	32	0x10000
A32 Pointer for I/Q Data	0x0C	32	0x0A000000
Buffer Size for I/Q Data	0x10	32	0x10000
A32 Pointer for Phase/Mag Data	0x14	32	0x0B000000
Buffer Size for Phase/Mag Data	0x18	32	0x10000

Register	Address	Data Width	Default (Ext.)	Ext. 53.1048MHz to 122.166MHz
Clock Control Register 0	0xA0	32	0x8186032	0x8184032
Clock Control Register 1	0xA4	32	0x8186032	0x8184032
Clock Control Register 2	0xA8	32	0x8186030	0x8184030
Clock Control Register 3	0xAC	32	0x6486030	0x6486030
Clock Control Register 4	0xB0	32	0x6486031	0x6486031
Clock Control Register 5	0xB4	32	0x10800AA	0x13500AA
Clock Control Register 6	0xB8	32	0x04B2030	0x04B26C1
Clock Control Register 7	0xBC	32	0xBD0037F	0xBD0037F
Clock Control Register 8	0xC0	32	0x40009D1	0x40009C3

# Registers: VME Interface

Register	Address	Data Width	Description
Channel Mask	0x00	8	Bits <7:0> - Set masks for Ch8 to Ch1 respectively. Bit <7> for Ch8, Bit <0> for Ch1. "1" = ON, "0" = OFF. Example: "00000001" means only Ch1 active.
DCDC Mode	0x01	8	Bits <1,0> - "00" - Fixed frequency; "01" - sweep 10% frequency; "1X" - spread spectrum. Default = "00".
VME IRQ Interrupt Level	0x02	8	Bits <2:0> - Hex number indicates the VME IRQ line. "000" = No interrupt "001" = IRQ1, "002" = IRQ2, ...
A32 Pointer for Raw Data	0x04	32	Indicates the starting address for ADC raw data in the A32 address space.
Channel Buffer Size for Raw Data	0x08	32	Indicates number of 32-bit words (two samples in each word) in memory reserved for each channel.
A32 Pointer for I/Q Data	0x0C	32	Indicates the starting address in memory for narrow band I and Q data.
Buffer Size for I/Q Data	0x10	32	Indicates number of 32-bit words in memory reserved for each channel.
A32 Pointer for Phase and Mag Data	0x14	32	Indicates the starting address in memory for narrow band phase and magnitude data.
Buffer Size for Phase and Mag Data	0x18	32	Indicates number of 32-bit words in memory reserved for each channel.
A24 Pointer for FPGA Flash Config Data	0x24	32	
Buffer Size for FPGA Flash Config Data	0x28	32	Indicates number of 32-bit words in memory reserved for each channel.
A24 Pointer for Flash Settings Data	0x2C	32	
Buffer Size for Flash Settings Data	0x30	32	Indicates number of 32-bit words in memory reserved for each channel.
VME A24 Pointer for Flash Data	0x34	32	
Buffer Size for Flash Data	0x38	32	Indicates number of 32-bit words in memory reserved for each channel.
Board ID (Read Only)	0x3C	32	Board ID, read only.

# Registers: Mode Control

Register	Address	Data Width	Description
Digitizer Mode	0x200	8	Bit <7> - '1' = external arm, '0' = soft arm; Bit <6> - '1' = external trigger, '0' = no trigger; Bit <5> - '1' = run under gate, '0' = no gate; Bit <4:2> - Unused; Bit <1> - '1' = DDC data ON, '0' = DDC data OFF; Bit <0> - '1' = Raw data ON, '0' = Raw data OFF.
Digitizer Switch	0x201	8	Bits <7:1> - Unused; Bit <0> - '1' = prevents digitizer from running.
Channel's Coupling Mode	0x202	8	Read only. Bits <7:0> - Denotes channels 8 to 1. Example: Bit <7> = Ch8. "0" - Transformers, "1" - Preamp.
Soft Arm	0x203	8	Bits <7:1> - Unused; Bit <0> - Set to '1' to arm digitizer when in soft arm mode. (0x200, bit <7> is '0'.)
Raw Data Sampling Rate	0x204	16	Bits <15:0> - Hex value is the sampling rate factor. $T_s = T_{min} * (Hex\_Value + 1)$ , where $T_{min} = 1 / clock\_rate$ .
Number of Triggers	0x208	32	Bits <23:0> - number of external triggers to take.
Number of Raw Samples	0x20C	32	Bits <23:0> - Number of samples or Number of Samples Per Trigger in trigger modes.
Read Current Number of Samples	0x210	32	Read only. Reads back number of samples processed on current trigger.
Read Current Number of Triggers	0x214	32	Read only. Reads back number of triggers processed on this run.
Block Count	0x218	32	Read only. Reads back number of runs taken.
Sync Delay	0x244	32	Bits <31:0> - Number of ADC clock cycles to delay after arm.
Trigger Delay	0x248	32	Bits <31:0> - Number of ADC clock cycles to delay after trigger.
Digitizer Busy	0x2AE	8	Bits <7:1> - Unused; Bit <0> - '1' = digitizer is busy, '0' - digitizer ready.
Firmware Version	0x2A8	32	Down Converter firmware named with version numbers starting with "F", i. e. x"F01".

# Registers: Down Converter

Register	Address	Data Width	Description
NCO Frequency	0x238	32	Bits <31:0> - Hex Input for the NCO, $F_o$ . Hex = $(F_o / F_s) * (2^{32})$ , where $F_s$ = sampling frequency.
CIC Decimation Rate	0x23C	16	Decimation rate of the CIC filter.
CIC Prescale	0x21E	8	Prescale factor for the input of the CIC filter. Gain = $1 / (2^{Reg})$ .
CIC Gain	0x23E	8	Gain adjustment for the output of the CIC filter. Gain = $2^{Reg}$ .
FIR 1 Gain	0x21F	8	Gain adjustment for the output of the FIR 1 filter. Gain = $2^{Reg}$ .
FIR 2 Gain	0x23F	8	Gain adjustment for the output of the FIR 2 filter. Gain = $2^{Reg}$ .
DDC Number of Samples	0x240	32	Bits <20:0> - Number of samples to save to memory from the digital down converter per channel.
DDC Output Mux	0x298	8	For firmware testing use only. Bits <3:0> - Mux select for the down converter output. x"0"= CIC output, x"1"= CIC Gain output, x"2"= FIR 1 output, x"3"= FIR 1 Gain output, x"4"= FIR 2 output, x"5"= FIR 2 Gain output, x"8"= NCO in-phase output, x"9"= raw data, x"A"= in-phase mixer output, x"B"= test pattern.
FIR 1 Coefficient Request	0x270	8	Bits <7:1> - Unused. Bit <0> - Request Bit for loading one new coefficient.
FIR 1 Coefficient Request End	0x271	8	Bits <7:1> - Unused. Bit <0> - Request End Bit after loading all new coefficients.
FIR 1 Coefficient Value	0x272	16	Bit <15> - Unused. Bits <14:0> - New FIR Coefficient value, 15 bits signed.
FIR 1 Coefficient Request	0x274	8	Bits <7:1> - Unused. Bit <0> - Request Bit for loading one new coefficient.
FIR 1 Coefficient Request End	0x275	8	Bits <7:1> - Unused. Bit <0> - Request End Bit after loading all new coefficients.
FIR 1 Coefficient Value	0x276	16	Bit <15> - Unused. Bits <14:0> - New FIR Coefficient value, 15 bits signed.

# Registers: Data Readout

Register	Address	Data Width	Description
Narrow Band Decimation Rate	0x21C	16	Bits <15:0> - Number of Magnitude and Intensity data points to skip. Unsigned.
Average Magnitude Ch1	0x250	16	Read only. Averaged magnitude from the down converter. Signed 16 bit word.
Average Magnitude Ch2	0x252	16	Read only. Averaged magnitude from the down converter. Signed 16 bit word.
Average Magnitude Ch3	0x254	16	Read only. Averaged magnitude from the down converter. Signed 16 bit word.
Average Magnitude Ch4	0x256	16	Read only. Averaged magnitude from the down converter. Signed 16 bit word.
Average Magnitude Ch5	0x258	16	Read only. Averaged magnitude from the down converter. Signed 16 bit word.
Average Magnitude Ch6	0x25A	16	Read only. Averaged magnitude from the down converter. Signed 16 bit word.
Average Magnitude Ch7	0x25C	16	Read only. Averaged magnitude from the down converter. Signed 16 bit word.
Average Magnitude Ch8	0x25E	16	Read only. Averaged magnitude from the down converter. Signed 16 bit word.
Accumulated Intensity Ch1 + Ch5	0x260	32	Read only. Accumulated Intensity Reading. Unsigned 32 bit word.
Accumulated Intensity Ch2 + Ch6	0x264	32	Read only. Accumulated Intensity Reading. Unsigned 32 bit word.
Accumulated Intensity Ch3 + Ch7	0x268	32	Read only. Accumulated Intensity Reading. Unsigned 32 bit word.
Accumulated Intensity Ch4 + Ch8	0x26C	32	Read only. Accumulated Intensity Reading. Unsigned 32 bit word.

# Registers: Interrupt

Register	Address	Data Width	Description
Software Set IRQ, #0 ~ #15	0x206	16	Bits <15:0> - IRQ15 ~ IRQ0. IRQ15 ~ IRQ12 not used in this design. Generate software interrupts by writing into register. Read back to see non-masked active interrupts (software or hardware generated).
VME IRQ Mask	0x290	16	Bits <11:0> - Mask for IRQ11 ~ IRQ0. "1" = Active, "0" = Disabled
IRQ Vector for IRQ #0	0x220	16	Active when ADC data out of range (any channel).
IRQ Vector for IRQ #1	0x222	16	Unassigned.
IRQ Vector for IRQ #2	0x224	16	Unassigned.
IRQ Vector for IRQ #3	0x226	16	Unassigned.
IRQ Vector for IRQ #4	0x228	16	Unassigned.
IRQ Vector for IRQ #5	0x22A	16	Unassigned.
IRQ Vector for IRQ #6	0x22C	16	Unassigned.
IRQ Vector for IRQ #7	0x22E	16	Unassigned.
IRQ Vector for IRQ #8	0x230	16	Unassigned.
IRQ Vector for IRQ #9	0x232	16	Real time Moving Average Magnitude and Integrated Intensity data points ready.
IRQ Vector for IRQ #10	0x234	16	Active at start of digitizer mode
IRQ Vector for IRQ #11	0x236	16	Active at end of digitizer mode

# Registers: ADC Overflow

Register	Address	Data Width	Description
ADC's OVR Status	0x2AD	8	Bits <7:0> - Denotes ADC data saturation for channels 8 to 1. Example: Bit <7> = Ch8. "1" = Overflow, "0" = Normal.
ADC 1 Abs Max Count	0x370	16	ADC data max count recorder for channel 1.
ADC 2 Abs Max Count	0x372	16	ADC data max count recorder for channel 2.
ADC 3 Abs Max Count	0x374	16	ADC data max count recorder for channel 3.
ADC 4 Abs Max Count	0x376	16	ADC data max count recorder for channel 4.
ADC 5 Abs Max Count	0x378	16	ADC data max count recorder for channel 5.
ADC 6 Abs Max Count	0x37A	16	ADC data max count recorder for channel 6.
ADC 7 Abs Max Count	0x37C	16	ADC data max count recorder for channel 7.
ADC 8 Abs Max Count	0x37E	16	ADC data max count recorder for channel 8.

# Registers: ADC Delays

Register	Address	Data Width	Description
ADC 1 Data Delay	0x140	8	Bits <4:0> - Data delay for channel 1, in ADC samples. Ranges from "0" to "31". Default is 16.
ADC 2 Data Delay	0x141	8	Bits <4:0> - Data delay for channel 2, in ADC samples. Ranges from "0" to "31". Default is 16.
ADC 3 Data Delay	0x142	8	Bits <4:0> - Data delay for channel 3, in ADC samples. Ranges from "0" to "31". Default is 16.
ADC 4 Data Delay	0x143	8	Bits <4:0> - Data delay for channel 4, in ADC samples. Ranges from "0" to "31". Default is 16.
ADC 5 Data Delay	0x144	8	Bits <4:0> - Data delay for channel 5, in ADC samples. Ranges from "0" to "31". Default is 16.
ADC 6 Data Delay	0x145	8	Bits <4:0> - Data delay for channel 6, in ADC samples. Ranges from "0" to "31". Default is 16.
ADC 7 Data Delay	0x146	8	Bits <4:0> - Data delay for channel 7, in ADC samples. Ranges from "0" to "31". Default is 16.
ADC 8 Data Delay	0x147	8	Bits <4:0> - Data delay for channel 8, in ADC samples. Ranges from "0" to "31". Default is 16.

# Registers: Sync Module

Register	Address	Data Width	Description
Time Stamp Counter	0x100	16	Read only. Sync with TCLK events. Bits <15:0> - Read back of time stamp counter.
TCLK Start Delay	0x102	16	Bits <15:0> - TCLK Start Delay.
TCLK Stop Delay	0x104	16	Bits <15:0> - TCLK Stop Delay.
TCLK Delay Scale	0x106	16	Bits <15:0> - TCLK Delay Scale.
BSYNC Start Delay	0x108	16	Bits <15:0> - BSYNC Start Delay.
BSYINC Stop Delay	0x10A	16	Bits <15:0> - BSYNC Stop Delay.
BSYNC Delay Scale	0x10C	16	Bits <15:0> - BSYNC Delay Scale.
TCLK Start Event	0x10E	8	Bits <7:0> - TCLK Start Event.
TCLK Stop Event	0x10F	8	Bits <7:0> - TCLK Stop Event.
BSYNC Start Event	0x110	8	Bits <7:0> - BSYNC Start Event.
BSYNC Stop Event	0x111	8	Bits <7:0> - BSYNC Stop Event.
SYNC In Source Mode	0x112	8	Bits <7:0> - Source for SYNC In signal. "0x0" = External Sync Signal, "0x1" = TCLK Start Event, "0x2" = TCLK Stop Event, "0x3" = BSYNC Start Event, "0x4" = BSYNC Stop Event.
Trigger Source Mode	0x113	8	Bits <7:0> - Source for Trigger signal. "0x0" = External Trigger Signal, "0x1" = TCLK Start Event, "0x2" = TCLK Stop Event, "0x3" = BSYNC Start Event, "0x4" = BSYNC Stop Event.
Gate Source Mode	0x114	8	Bits <7:0> - Source for Gate signal. "0x0" = External Gate Signal, "0x1" = TCLK Start/Stop Event, "0x2" = BSYNC Start/Stop Event.
SYNC Out Source Mode	0x115	8	Bits <7:0> - Source for Sync Out port. "0x0" = External Sync In, "0x1" = External Trigger, "0x2" = External Gate, "0x3" = TCLK Start Event, "0x4" = TCLK Stop Event, "0x5" = BSYNC Start Event, "0x6" = BSYNC Stop Event, "0x7" = ADC samples, "0x8" = Mode Active, "0x9" = ADC's clock, "0xA" = ATF-NB gate, "0xB" = ATF-WB gates, "0xC" = TBT gate, "0xD" = Turn Marker.

# Registers: Sync IRQ

Register	Address	Data Width	Description
SYNC IRQ Mask	0x118	16	Bits <8:0> - Mask for SYNC IRQ8 ~ IRQ0. "1" = Active, "0" = Disabled
Software Set SYNC IRQ	0x11A	16	Bits <15:0> - SYNC IRQ15 ~ IRQ0. IRQ15 ~ IRQ9 not used in this design. Generate software interrupts by writing into register. Read back to see non-masked active interrupts (software or hardware generated).
IRQ Vector for IRQ #0	0x120	16	Active on external Sync Signal.
IRQ Vector for IRQ #1	0x122	16	Active on external Trigger signal.
IRQ Vector for IRQ #2	0x124	16	Active on external Gate signal positive edge.
IRQ Vector for IRQ #3	0x126	16	Active on external Gate signal negative edge.
IRQ Vector for IRQ #4	0x128	16	Active on TCLK Start event.
IRQ Vector for IRQ #5	0x12A	16	Active on TCLK Stop event.
IRQ Vector for IRQ #6	0x12C	16	Active on BSYNC Start event.
IRQ Vector for IRQ #7	0x12E	16	Active on BSYNC Stop event.
IRQ Vector for IRQ #8	0x130	16	Active on TCLK time stamp counter reset.

# Registers: ADC Chip 1

Register	Address	Data Width	Description
Power Down Modes Reg. A	0x80	16	<p>Bits &lt;9:6&gt; - Not Used. Must be "0". Bit &lt;10&gt; - Software Reset. "1" resets all internal registers and self-clears to "0".</p> <p>Bit &lt;5&gt; - Reference. "0"=Internal Reference Enabled, "1"=External Reference Enabled.</p> <p>Bits &lt;4:1&gt; - Channels 4 ~ 1 Power Down. "1"=Power Down, "0"=Normal Operation.</p> <p>Bit &lt;0&gt; - Global Power Down, including channels 1 ~ 4. "1"=Power Down, "0"=Normal Operation.</p>
Input Clock Gain Reg. B	0x82	16	<p>Bits &lt;10:7, 1:0&gt; - Not Used. Must be "0".</p> <p>Bits &lt;6:2&gt; - CLKIN Gain. "11000"= Gain 0, minimum gain, "00000"= Gain 1, default gain after reset, "01100"= Gain 2, "01010"= Gain 3, "01001"= Gain 4, "01000"= Gain 5, maximum gain.</p>
Capture Test Pattern Reg. C	0x84	16	<p>Bits &lt;10, 8, 4:0&gt; - Not Used. Must be "0". Bit &lt;9&gt; - Data Format Selection. "0" = 2's Complement format, "1" = Straight binary format</p> <p>Bits &lt;7:5&gt; - Capture Test Patterns. "000"= Normal ADC operation, "001"= Output all zeros, "010"= Output all ones, "011"= Output toggle pattern, "100"= Unused, "101"= Output custom pattern (contents of CUSTOM pattern registers 0x86 and 0x88), "110"= Output DESKEW pattern (serial stream of 1010...), "111"= Output SYNC pattern.</p>
Test Patterns Reg. D	0x86	16	<p>Bits &lt;10:0&gt; - Lower 11 bits of custom pattern. "D10 D9 D8 ... D0"</p>
Fine Gain Reg. E	0x88	16	<p>Bits &lt;2:0&gt; - Upper 3 bits of custom pattern, "D13 D12 D11".</p> <p>Bits &lt;7:3&gt; - Not Used. Must be "0".</p> <p>Bits &lt;10:8&gt; - Fine Gain Control. "000"= 0dB Gain (full-scale range=2.00VPP), "001"= 1dB Gain (full-scale range=1.78VPP), "010"= 2dB Gain (full-scale range=1.59VPP), "011"= 3dB Gain (full-scale range=1.42VPP), "100"= 4dB Gain (full-scale range=1.26VPP), "101"= 5dB Gain (full-scale range=1.12VPP), "110"= 6dB Gain (full-scale range=1.00VPP).</p>

# Registers: ADC Chip 1 cont.

Register	Address	Data Width	Description
Output Data Config. Reg. F	0x8A	16	<p>Bit &lt;10&gt; - Over-Ride Bit. All the functions in this register can also be controlled using the parallel control pins. By setting this bit to "1", the contents of register will over-ride the settings of the parallel pins. Bits &lt;9:8, 3&gt; - Not Used. Must be "0".</p> <p>Bit &lt;7&gt; - Byte/bit Wise outputs. "0": Byte wise, "1": bit wise.</p> <p>Bit &lt;6&gt; - MSB or LSB First Selection. "0": MSB First, "1": LSB First.</p> <p>Bit &lt;5&gt; - Coarse Gain Control. "0"=0dB Coarse Gain (full-scale range=2.0 VPP), "1"=3.5dB Coarse Gain (full-scale range=1.34 VPP)</p> <p>Bit &lt;4&gt; - Bit Clock Capture Edge (only when SDR bit clock is selected, Bit 1 = "1"). "0"=Capture data with falling edge of bit clock, "1"=Capture data with rising edge of bit clock.</p> <p>Bit &lt;2&gt; - Serialization Factor Selection. "0"=14x Serialization, "1"=16x Serialization.</p> <p>Bit &lt;1&gt; - Bit Clock Selection (only in 2-wire interface). "0"=DDR Bit Clock, "1"=SDR Bit Clock.</p> <p>Bit &lt;0&gt; - Interface Selection. "0"=1 Wire interface, "1"=2 Wire interface.</p>
Data Interface Reg. G	0x8C	16	<p>Bit &lt;0&gt; - LVDS Current Double For Data Outputs. "0"=Nominal LVDS current, as set by Bits &lt;5:2&gt;. "1"=Double the nominal value.</p> <p>Bit &lt;1&gt; - LVDS Current Double for Bit and Word Clock Outputs. "0"=Nominal LVDS current, as set by Bits&lt;5:2&gt;. "1"=Double the nominal value.</p> <p>Bits &lt;3:2&gt; - LVDS Current Setting for Data Outputs. "00"= 3.5mA, "01"= 4mA, "10"= 2.5mA, "11"= 3mA;</p> <p>Bits &lt;5:4&gt; - CVDS Current Setting For Bit and Word Clock Outputs. "00"= 3.5mA, "01"= 4mA, "10"= 2.5mA, "11"= 3mA;</p> <p>Bits &lt;10:6&gt; - LVDS Internal Termination For Bit and Word Clock outputs. "00000"= No internal termination, "00001"= 166 Ω, "00010"= 200 Ω, "00100"= 250 Ω, "01000"= 333 Ω, "10000"= 500 Ω; Any combination of above bits can be programmed, resulting in a parallel combination of the selected values. For example, "00101" is the parallel combination of 166     250=100 Ω. "00101"= 100 Ω</p>
Data Interface Reg. H	0x8E	16	<p>Bits &lt;10:9&gt; - Only when 2-wire interface is selected. "00" Byte-wise or bitwise output, 1x frame clock, "11" Word-wise output enabled, 0.5x frame clock.</p> <p>Bits &lt;8:5&gt; - Not Used. Must be "0".</p> <p>Bits &lt;4:0&gt; - LVDS Internal Termination For Data Outputs. "00000"= No internal termination, "00001"= 166 Ω, "00010", 200 Ω, "00100"= 250 Ω, "01000"= 333 Ω, "10000"= 500 Ω</p> <p>Any combination of above bits can be programmed, resulting in a parallel combination of the selected values. For example, "00101" is the parallel combination of 166     250=100 Ω, "00101"= 100 Ω</p>

# Registers: ADC Chip 2

Register	Address	Data Width	Description
Power Down Modes Reg. A	0x90	16	<p>Bits &lt;9:6&gt; - Not Used. Must be "0". Bit &lt;10&gt; - Software Reset. "1" resets all internal registers and self-clears to "0".</p> <p>Bit &lt;5&gt; - Reference. "0"=Internal Reference Enabled, "1"=External Reference Enabled.</p> <p>Bits &lt;4:1&gt; - Channels 4 ~ 1 Power Down. "1"=Power Down, "0"=Normal Operation.</p> <p>Bit &lt;0&gt; - Global Power Down, including channels 1 ~ 4. "1"=Power Down, "0"=Normal Operation.</p>
Input Clock Gain Reg. B	0x92	16	<p>Bits &lt;10:7, 1:0&gt; - Not Used. Must be "0".</p> <p>Bits &lt;6:2&gt; - CLKIN Gain. "11000"= Gain 0, minimum gain, "00000"= Gain 1, default gain after reset, "01100"= Gain 2, "01010"= Gain 3, "01001"= Gain 4, "01000"= Gain 5, maximum gain.</p>
Capture Test Pattern Reg. C	0x94	16	<p>Bits &lt;10, 8, 4:0&gt; - Not Used. Must be "0". Bit &lt;9&gt; - Data Format Selection. "0" = 2's Complement format, "1" = Straight binary format</p> <p>Bits &lt;7:5&gt; - Capture Test Patterns. "000"= Normal ADC operation, "001"= Output all zeros, "010"= Output all ones, "011"= Output toggle pattern, "100"= Unused, "101"= Output custom pattern (contents of CUSTOM pattern registers 0x96 and 0x98), "110"= Output DESKEW pattern (serial stream of 1010...), "111"= Output SYNC pattern.</p>
Test Patterns Reg. D	0x96	16	<p>Bits &lt;10:0&gt; - Lower 11 bits of custom pattern. "D10 D9 D8 ... D0"</p>
Fine Gain Reg. E	0x98	16	<p>Bits &lt;2:0&gt; - Upper 3 bits of custom pattern, "D13 D12 D11".</p> <p>Bits &lt;7:3&gt; - Not Used. Must be "0".</p> <p>Bits &lt;10:8&gt; - Fine Gain Control. "000"= 0dB Gain (full-scale range=2.00VPP), "001"= 1dB Gain (full-scale range=1.78VPP), "010"= 2dB Gain (full-scale range=1.59VPP), "011"= 3dB Gain (full-scale range=1.42VPP), "100"= 4dB Gain (full-scale range=1.26VPP), "101"= 5dB Gain (full-scale range=1.12VPP), "110"= 6dB Gain (full-scale range=1.00VPP).</p>

# Registers: ADC Chip 2 cont.

Register	Address	Data Width	Description
Output Data Config. Reg. F	0x9A	16	<p>Bit &lt;10&gt; - Over-Ride Bit. All the functions in this register can also be controlled using the parallel control pins. By setting this bit to "1", the contents of register will over-ride the settings of the parallel pins. Bits &lt;9:8, 3&gt; - Not Used. Must be "0".</p> <p>Bit &lt;7&gt; - Byte/bit Wise outputs. "0": Byte wise, "1": bit wise.</p> <p>Bit &lt;6&gt; - MSB or LSB First Selection. "0": MSB First, "1": LSB First.</p> <p>Bit &lt;5&gt; - Coarse Gain Control. "0"=0dB Coarse Gain (full-scale range=2.0 VPP), "1"=3.5dB Coarse Gain (full-scale range=1.34 VPP)</p> <p>Bit &lt;4&gt; - Bit Clock Capture Edge (only when SDR bit clock is selected, Bit 1 = "1"). "0"=Capture data with falling edge of bit clock, "1"=Capture data with rising edge of bit clock.</p> <p>Bit &lt;2&gt; - Serialization Factor Selection. "0"=14x Serialization, "1"=16x Serialization.</p> <p>Bit &lt;1&gt; - Bit Clock Selection (only in 2-wire interface). "0"=DDR Bit Clock, "1"=SDR Bit Clock.</p> <p>Bit &lt;0&gt; - Interface Selection. "0"=1 Wire interface, "1"=2 Wire interface.</p>
Data Interface Reg. G	0x9C	16	<p>Bit &lt;0&gt; - LVDS Current Double For Data Outputs. "0"=Nominal LVDS current, as set by Bits &lt;5:2&gt;. "1"=Double the nominal value.</p> <p>Bit &lt;1&gt; - LVDS Current Double for Bit and Word Clock Outputs. "0"=Nominal LVDS current, as set by Bits&lt;5:2&gt;. "1"=Double the nominal value.</p> <p>Bits &lt;3:2&gt; - LVDS Current Setting for Data Outputs. "00"= 3.5mA, "01"= 4mA, "10"= 2.5mA, "11"= 3mA;</p> <p>Bits &lt;5:4&gt; - CVDS Current Setting For Bit and Word Clock Outputs. "00"= 3.5mA, "01"= 4mA, "10"= 2.5mA, "11"= 3mA;</p> <p>Bits &lt;10:6&gt; - LVDS Internal Termination For Bit and Word Clock outputs. "00000"= No internal termination, "00001"= 166 Ω, "00010"= 200 Ω, "00100"= 250 Ω, "01000"= 333 Ω, "10000"= 500 Ω; Any combination of above bits can be programmed, resulting in a parallel combination of the selected values. For example, "00101" is the parallel combination of 166     250=100 Ω. "00101"= 100 Ω</p>
Data Interface Reg. H	0x9E	16	<p>Bits &lt;10:9&gt; - Only when 2-wire interface is selected. "00" Byte-wise or bitwise output, 1x frame clock, "11" Word-wise output enabled, 0.5x frame clock.</p> <p>Bits &lt;8:5&gt; - Not Used. Must be "0".</p> <p>Bits &lt;4:0&gt; - LVDS Internal Termination For Data Outputs. "00000"= No internal termination, "00001"= 166 Ω, "00010", 200 Ω, "00100"= 250 Ω, "01000"= 333 Ω, "10000"= 500 Ω</p> <p>Any combination of above bits can be programmed, resulting in a parallel combination of the selected values. For example, "00101" is the parallel combination of 166     250=100 Ω, "00101"= 100 Ω</p>

# Registers: Clock Driver

Register	Address	Data Width	Description
Control Register 0 (Output Divider 0)	0xA0	32	<p>Bits &lt;0:1&gt; - Pre-Divider selection for primary reference. "00" = 3-state, "01" = divide by 1, "10", divide by 2, "11" = reserved.</p> <p>Bits &lt;4:5&gt; - Output Mux 0 Select. "00" = PRI_IN (On board oscillator), "01" = SEC_IN (External clock), "10" = SMART_MUX, "11" = VCO_CORE.</p> <p>Bits &lt;12:6&gt; - Coarse phase adjust select for output 0. Bits &lt;19:13&gt; - Output Divider 0 Ratio Select. Bit &lt;20&gt; - "1" = output 0 enabled, "0" = disabled.</p> <p>Bit &lt;21&gt; - High swing LVPEC when set to "1", normal swing when set to "0". Bits &lt;3:2&gt; - Reserved. Bits &lt;26:27&gt; - Output buffer select 0.</p> <p>Bits &lt;22:23&gt; - LVCMOS mode select for Output 0 positive pin. "00" = Active, "10" = Inverting, "11" = Low, "01" = 3-state.</p> <p>Bits &lt;24:25&gt; - LVCMOS mode select for Output 0 negative pin. "00" = Active, "10" = Inverting, "11" = Low, "01" = 3-state.</p>
Control Register 1 (Output Divider 1)	0xA4	32	<p>Bits &lt;0:1&gt; - Pre-Divider selection for secondary reference. "00" = 3-state, "01" = divide by 1, "10", divide by 2, "11" = reserved.</p> <p>Bits &lt;4:5&gt; - Output Mux 1 Select. "00" = PRI_IN (On board oscillator), "01" = SEC_IN (External clock), "10" = SMART_MUX, "11" = VCO_CORE.</p> <p>Bits &lt;12:6&gt; - Coarse phase adjust select for output 1. Bits &lt;19:13&gt; - Output Divider 1 Ratio Select. Bit &lt;20&gt; - "1" = output 1 enabled, "0" = disabled.</p> <p>Bit &lt;21&gt; - High swing LVPEC when set to "1", normal swing when set to "0". Bits &lt;3:2&gt; - Reserved. Bits &lt;26:27&gt; - Output buffer select 1.</p> <p>Bits &lt;22:23&gt; - LVCMOS mode select for Output 1 positive pin. "00" = Active, "10" = Inverting, "11" = Low, "01" = 3-state.</p> <p>Bits &lt;24:25&gt; - LVCMOS mode select for Output 1 negative pin. "00" = Active, "10" = Inverting, "11" = Low, "01" = 3-state.</p>
Control Register 2 (Output Divider 2)	0xA8	32	<p>Bit&lt;0&gt; - Reference divider bit 0. Bit&lt;1&gt; - Reference divider bit 1. Bits &lt;3:2&gt; - Reserved. Bits &lt;26:27&gt; - Output buffer select 2.</p> <p>Bits &lt;4:5&gt; - Output Mux 2 Select. "00" = PRI_IN (On board oscillator), "01" = SEC_IN (External clock), "10" = SMART_MUX, "11" = VCO_CORE.</p> <p>Bits &lt;12:6&gt; - Coarse phase adjust select for output 2. Bits &lt;19:13&gt; - Output Divider 2 Ratio Select. Bit &lt;20&gt; - "1" = output 2 enabled, "0" = disabled.</p> <p>Bit &lt;21&gt; - High swing LVPEC when set to "1", normal swing when set to "0".</p> <p>Bits &lt;22:23&gt; - LVCMOS mode select for Output 2 positive pin. "00" = Active, "10" = Inverting, "11" = Low, "01" = 3-state.</p> <p>Bits &lt;24:25&gt; - LVCMOS mode select for Output 2 negative pin. "00" = Active, "10" = Inverting, "11" = Low, "01" = 3-state.</p>
Control Register 3 (Output Divider 3)	0xAC	32	<p>Bit&lt;0&gt; - Reference divider bit 2. Bits &lt;3:1&gt; - Reserved. Bits &lt;26:27&gt; - Output buffer select 3.</p> <p>Bits &lt;4:5&gt; - Output Mux 3 Select. "00" = PRI_IN (On board oscillator), "01" = SEC_IN (External clock), "10" = SMART_MUX, "11" = VCO_CORE.</p> <p>Bits &lt;12:6&gt; - Coarse phase adjust select for output 3. Bits &lt;19:13&gt; - Output Divider 3 Ratio Select. Bit &lt;20&gt; - "1" = output 3 enabled, "0" = disabled.</p> <p>Bit &lt;21&gt; - High swing LVPEC when set to "1", normal swing when set to "0".</p> <p>Bits &lt;22:23&gt; - LVCMOS mode select for Output 3 positive pin. "00" = Active, "10" = Inverting, "11" = Low, "01" = 3-state.</p> <p>Bits &lt;24:25&gt; - LVCMOS mode select for Output 3 negative pin. "00" = Active, "10" = Inverting, "11" = Low, "01" = 3-state.</p>

# Registers: Clock Driver cont.

Register	Address	Data Width	Description
Control Register 4 (Output Divider 4)	0xB0	32	<p>Bit&lt;0&gt; - Reserved, must be set to "1". Bits &lt;3:1&gt; - Reserved.</p> <p>Bits &lt;4:5&gt; - Output Mux 4 Select. "00" = PRI_IN (On board oscillator), "01" = SEC_IN (External clock), "10" = SMART_MUX, "11" = VCO_CORE.</p> <p>Bits &lt;12:6&gt; - Coarse phase adjust select for output 4. Bits &lt;19:13&gt; - Output Divider 4 Ratio Select. Bit &lt;20&gt; - "1" = output 4 enabled, "0" = disabled.</p> <p>Bit &lt;21&gt; - High swing LVPEC when set to "1", normal swing when set to "0". Bits &lt;26:27&gt; - Output buffer select 4.</p> <p>Bits &lt;22:23&gt; - LVCMOS mode select for Output 4 positive pin. "00" = Active, "10" = Inverting, "11" = Low, "01" = 3-state.</p> <p>Bits &lt;24:25&gt; - LVCMOS mode select for Output 4 negative pin. "00" = Active, "10" = Inverting, "11" = Low, "01" = 3-state.</p>
Control Register 5	0xB4	32	<p>Bits &lt;0:1&gt; - Input buffer select. "01" = LVPECL, "11" = LVDS, "00" = LVCMOS. Bits &lt;2:4&gt; - EEPROM clock select. Bit &lt;5&gt; - EEPROM clock select enable.</p> <p>Bit &lt;6&gt; - Input buffer termination. "1" = DC, "0" = AC. Bit &lt;7&gt; - Input buffers hysteresis enable, "1" recommended.</p> <p>Bit &lt;8&gt; - Primary input termination. "0" = enable, "1" = disable. Bit &lt;9&gt; - Primary input negative pin biased with internal Vbb voltage when set to "1".</p> <p>Bit &lt;10&gt; - Secondary input negative pin biased with internal Vbb voltage when set to "1". Bits &lt;13:12&gt; - Reserved, must be "0".</p> <p>Bit &lt;11&gt; - Fail Safe is enabled for all input buffers when set to "1", DC coupling only. Bits &lt;21:14&gt; - Input Divider settings.</p> <p>Bits &lt;25:22&gt; - Lock-detect window width. "0000" = Narrow window, "0001", "0010", "0100", "0101", ... 1110" = Widest window, "XX11" = Reserved.</p> <p>Bit &lt;26&gt; - "0" = triggers after first lock detection, "1" = triggers after 64 cycles of lock detection.</p> <p>Bit &lt;27&gt; - "0" selects digital PLL_Lock 0, "1" selects digital PLL_Lock 1.</p>
Control Register 6	0xB8	32	<p>Bit &lt;0&gt; - VCO select, "0": VCO1 (low range), "1": VCO2 (high range). Bits &lt;2:1&gt; - Pre-scaler setting. Bits &lt;23, 11&gt; - Reserved, must be set to "0".</p> <p>Bits &lt;15:13&gt; - Bypass Divider setting. Bits &lt;10:3&gt; - Feedback Divider setting. Bit &lt;26&gt; - "1" = External loop filter is used, "0" = Internal loop filter is used.</p> <p>Bit &lt;12&gt; - "0" = Secondary input buffer internal termination enabled, "1" = Secondary internal termination circuitry disabled.</p> <p>Bit &lt;20&gt; - "0" = outputs synchronized to reference input on low-to-high pulse on SYNC pin, "1" = outputs synchronized to SYNC high-to-low pulse.</p> <p>Bit &lt;21&gt; - "1" = Wide pulse, "0" = Narrow pulse. Bit &lt;22&gt; - Enable VCO calibration command. Bit &lt;24&gt; - Enable auxiliary output when set to "1".</p> <p>Bit &lt;25&gt; - Select the output that will drive AUX output. "0" = Output divider 2, "1" = divider 3.</p> <p>Bit &lt;27&gt; - "1": Calibration mode = Manual mode, "0": Calibration mode = startup mode. Bits &lt;19:16&gt; - Charge Pump current select.</p>
Control Register 7	0xBC	32	<p>Bits &lt;20:0&gt; - Loop filter control setting. Bit &lt;21&gt; - Reserved, must be set to "0". Bits &lt;24, 22&gt; - Diagnostics, set to "1".</p> <p>Bits &lt;25, 23&gt; - Smart Mux. "0" enables short delay for fast operation, "1" for long delay. Bit &lt;26&gt; - Read only. "0" = EEPROM unlock. "1" = EEPROM locked.</p> <p>Bit &lt;27&gt; - Reserved, always reads "1".</p>

# Registers: Clock Driver cont.

Register	Address	Data Width	Description
Control Register 8	0xC0	32	<p>Bits &lt;5:0&gt; - Calibration read back from device.            Bit &lt;6&gt; - Read only, status of the PLL lock pin driven by the device.            Bit &lt;7&gt; - "0" = Set device Sleep mode ON, "1" = Normal mode.            Bit &lt;8&gt; - "0" = Forces /SYNC, "1" = exit Sync.            Bits &lt;20, 13, 9&gt; - Reserved, must be set to "0".            Bits &lt;12:10&gt; - Silicon Revision.            Bits &lt;24:21, 19:14&gt; - Factor registers.            Bits &lt;27:24&gt; - Synthesizer Source Indicator.</p>
Unlock CDCE62005	0xC4	8	Write Only. Bit <0> - Unlock CDCE62005.
Lock CDCE62005	0xC5	8	Write Only. Bit <0> - Copy data from RAM to EEPROM. Use discouraged.
Oscillator Enable	0xC6	8	Bit <0> - "1" - Enable internal oscillator for ADC clock.
Clock Reference Select	0xC7	8	Bit <0> - By pin, optional to SPI
Clock Base SYNC	0xC8	8	Bit <0> - By pin, optional to SPI
Clock Base Power Down	0xC9	8	Bit <0> - By pin, optional to SPI
Clock Base PLL Lock	0xCA	8	Bit <0> - "1" - PLL locked.

# Registers: Flash

Register	Address	Data Width	Description
Write Enable	0x160	8	Write command to enable write ops to Flash.
Write Disable	0x161	8	Write command to disable write ops to Flash.
Read/Write Status	0x162	8	Read/Write to Flash status register.
Erase Bulk	0x163	8	Write command to erase bulk in Flash.
Read Flash Chip ID	0x164	8	Read Flash ID.
Erase Sector	0x168	32	Write command to erase sector of Flash. Bits <23:0> - Number of sectors.

# Registers: Remote Update

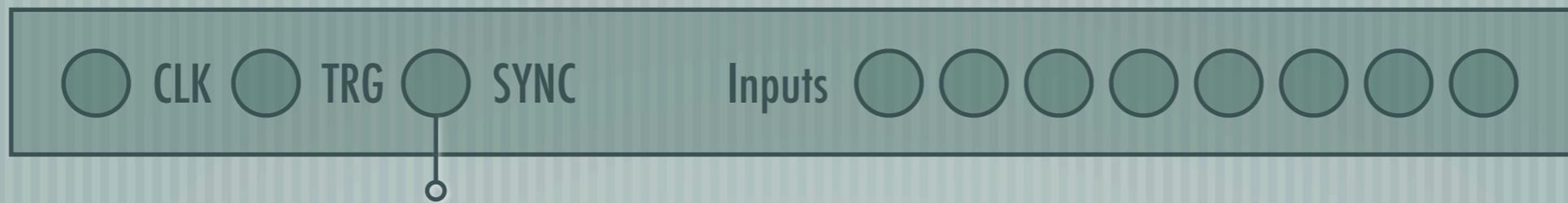
Register	Address	Data Width	Description
Read Master State Machine (MSM) Current State Mode	0x180	8	NA
Read Past Status 1 MSM Mode	0x181	8	NA
Read Current Application Mode Watch Dog Enable	0x182	8	NA
Read Past Status 1 Reconfiguration Trigger Conditions Source	0x183	8	NA
Read Past Status 2 MSM Mode	0x184	8	NA
Read Past Status 2 Reconfiguration Trigger Conditions Source	0x185	8	NA
R/W the Early Conf_Done Check	0x186	8	NA
R/W Watchdog Enable Value	0x187	8	NA
R/W The Osc_Internal Option	0x188	8	NA
R/W Watchdog Timeout Value	0x18A	16	NA
Read Current Application Mode Watchdog Time Value	0x18C	32	NA
Read Past Status 1 Boot Address	0x190	32	NA
Read Past Status 2 Boot Address	0x194	32	NA
R/W Boot Address (Upper 22 bits of 24 bit address value)	0x198	32	NA
Read Current Factory Mode Boot Address 24 bit	0x19C	32	NA
Write the Command to Reconfigure FPGA	0x1A0	8	NA
Write the Command to Reset Watchdog Timer	0x1A6	8	NA

# Registers: Generic

Register	Address	Data Width	Description
Generic Register 0	0x60	32	Generic register.
Generic Register 1	0x64	32	Generic register.
Generic Register 2	0x68	32	Generic register.
Generic Register 3	0x6C	32	Generic register.
Generic Register 4	0x70	32	Generic register.
Generic Register 5	0x74	32	Generic register.
Generic Register 6	0x78	32	Generic register.
Generic Register 7	0x7C	32	Generic register.

# Connectors and Switches

Digitizer Front Panel



Used as external arm

Hardware A16 Address Switches:

(Ignore this label here)

