

TDUControl Changes and Auto-Learn

Evan Niner

5/29/13

TDU Firmware Upgrade

- Last week at Ash River Peter upgraded the TDU ARM firmware to version 1.6 on the master and slaves of both timing chains.
- One feature of this upgrade is two new ARM commands: LCD_STATUS and PROG_STATUS. They are described in doc-9106.
- LCD_STATUS returns the current color of the front panel lcd screen and which screen is being displayed.
- PROG_STATUS returns the FGGA boot prom programming status and the last accessed page of the boot prom.

TDUControl Upgrade

- The gui has been modified to include two buttons in the firmware tab to read this information.
- The results are currently displayed in hex in the response tab. The key is in the firmware documentation.
- I will modify this to print in a more user friendly fashion.
- This is now available in the FD02_02_03 test release.

The screenshot displays the TDU Control Interface GUI. At the top, the window title is "TDU Control Interface". Below the title bar is a menu bar with "File", "Config", "Timing", "Info", and "About". A "Server" dropdown menu is set to "TDU-Master-ARM-02", with "Connect" and "Disconnect" buttons. The status bar shows "Sending LCD Status Request" and "Connected", with a message "LCD Status read successful" on the right.

The main display area is divided into two sections. The top section is a status table:

TDU Status	Master Timing Unit	Voltage	5.152	Delay	0 ns	GPS Lock	<input checked="" type="checkbox"/>
Serial No.	0x1592aa49	Current	0.860618	Delay Top	0 ns	GPS Satellites	10
Software Ver.	1.6	Temp	25.5625	Delay Side	0 ns	Heart Beats	<input type="checkbox"/>
Firmware Ver	2.14	Run Control	Unknown			Timing Pings	<input type="checkbox"/>
FPGA State	Booted	Control	0x0000	TDU Errors 1	0x0000	Run Number	0
Time of Last Sync	-	Status	0x0008	TDU Errors 2	0x0000	Partition	-1

The bottom section is the "Firmware" tab, which contains a "Command" panel with buttons for "Ping", "Status", "Ident", "GPS Stat", "Reload GPS", "Buffer Data", "Unlock FPGA", "Lock FPGA", "Erase FPGA", "Boot FPGA", "Read Page", "Write Page", "LCD Status", and "Prog Status". The "LCD Status" and "Prog Status" buttons are circled in blue. Below the command panel are "Read Reg." and "Write Reg." buttons, and input fields for "Register/Page:" (0x0) and "Value:" (0x0). The "Response" panel on the right shows "TDU Response" with a "Clear" button and two lines of hex data circled in blue: "Data: 0x01 0x00 0x00 0x2a" and "Data: 0x00 0xe0 0x2a". At the bottom right, there is a "Firmware Image:" field with a "Browse..." button and a "Download Firmware" button.

Auto-learn Delay Calculation

- I have been exercising the auto-learn feature of the TDU to calculate delays in the timing chain.
- Some important notes:
 - Timing chain 1 and 2 are both now being terminated after stdu-10 because there have been issues loading firmware onto stdu-11 previously reported.
 - In order to get delay calculations for a dcm chain a loop-back connector must be put in place at the end of the chain. These were found to have been missing. Rick corrected this for diblocks 1-6 and the side dcms on 7-8. This has been noted for future dcm installation. If a connector has not been added the dcm chain will return a delay value in excess of 500,000 ns indicating a timeout.
 - In order for an individual dcm to store a delay value it must be programmed to listen to external signal from a given timing chain. When a run is not in progress dcms are not set to listen to external signals. This must be done manually right now. Running auto-learn from TDUControl will calculate the delays properly and set the TDU delay registers but not the DCM delay registers without this step.

TDU	Delay Type	Delay (ns)
Mtdu-01	backbone	1369.1875
""	Top DCM chain	n/a
""	Side DCM chain	n/a
Stdu-01-01	backbone	859.375
""	Top DCM chain	4546.875
""	Side DCM chain	4546.875
Stdu-01-02	backbone	765.625
""	Top DCM chain	4453.125
""	Side DCM chain	4453.125
Stdu-01-03	backbone	671.875
""	Top DCM chain	4359.375
""	Side DCM chain	4359.375
Stdu-01-4	backbone	578.125
""	Top DCM chain	4265.625
""	Side DCM chain	4265.625

Delays are calculated as time-of-flight/2 so the delays are smallest closest to the loop-back.

Time between the slaves follows a pattern of being 93.75 ns (12 clock ticks) different. The cable between slaves is 38' at 1.5 ft/ns. The internal delays are not known so I do not have exact expectation values to compare to.

DCM chain delays are:

$$\text{Delay} = \text{DCM_offset} + \text{TDU_tof}/2 - \text{DCM_tof}/2$$

The DCM offset is a default of 4000 ns currently, this can be changed.

Timing chain 2 reports the same delay values as timing chain 1.

DCM	Delay (ns)
1	7.8125
2	46.875
3	85.9375
4	132.8125
5	171.875
6	210.9375
7	210.9375
8	171.875
9	132.8125
10	85.9375
11	46.875
12	7.8125

I checked the individual delay registers within the timing chain. This was done on chain 1 only.

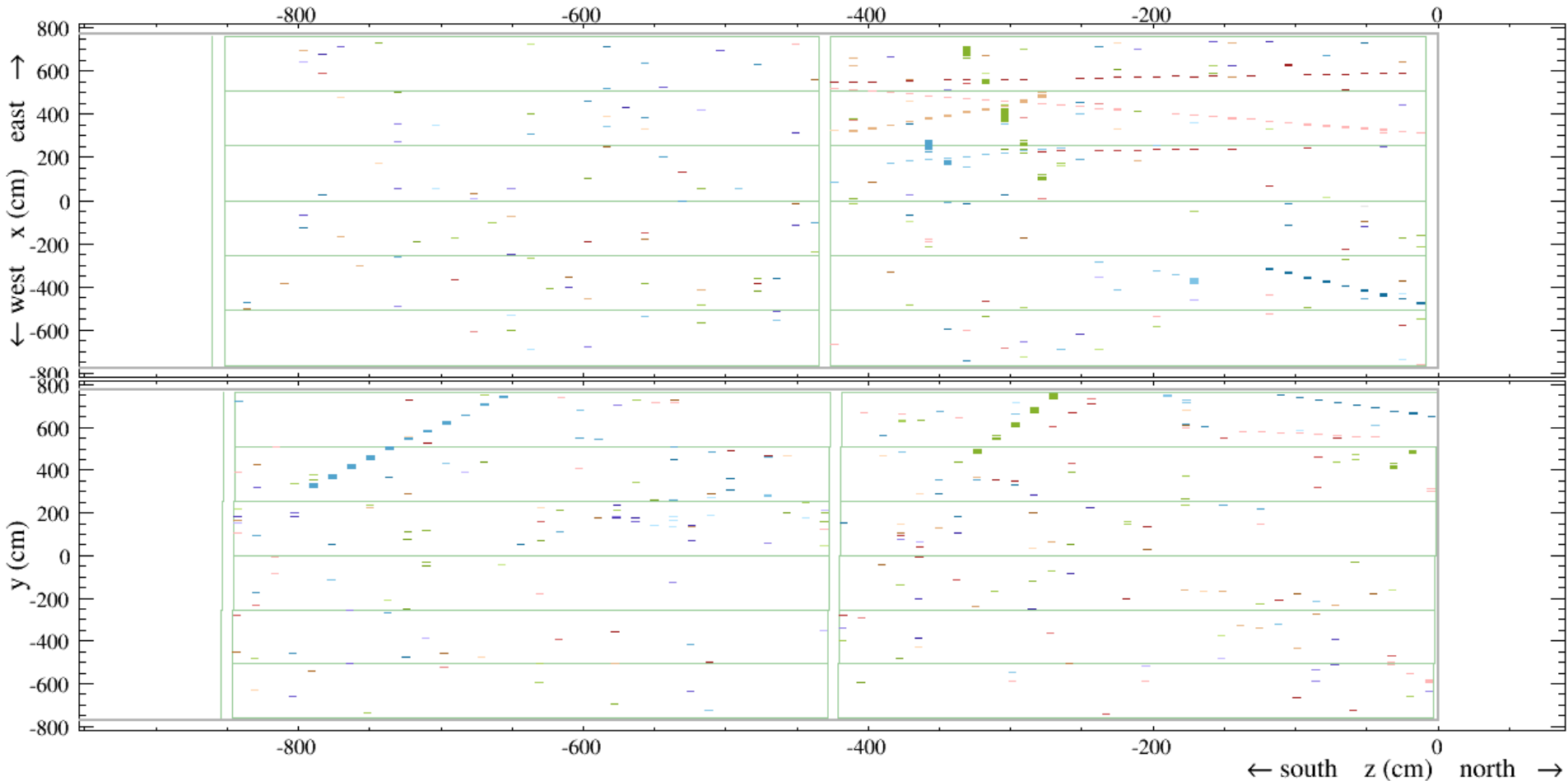
The table shown on the left is for diblock 1. I also examined the dcm delays in diblocks 4-6 and found the same values (one dcm on diblock 6 differed by 1 clock tick).

Event Display

Taken at 12:50 PM Central 5/29/13 during current run.

Pink track in XZ is not fully present in YZ and brown track is missing.

Looking though a number of events most tracks look to be in time, but some missing such as this one. A more detailed investigation is needed.



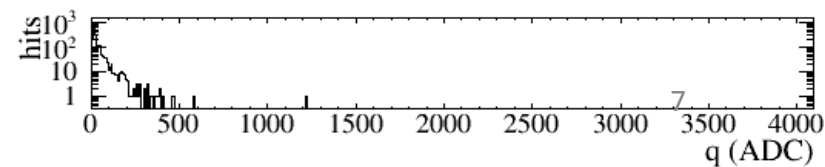
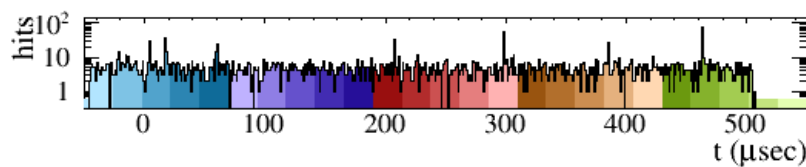
NOvA - FNAL E929

Run: 10342 / 2

Event: 45868 / CAL

UTC Wed May 29, 2013

17:52:59.661492992



Summary

- TDU firmware and monitoring gui have been updated to allow monitoring of the front panel display screens.
- Delays are being properly calculated for the tdu chains, and storing the delay values in dcms is also possible.
- Currently all delays are still being set to 0. Do we want to change this now since the views still look by eye to be out of synch in some cases?
- I will be at Ash River June 2-14 if any work needs to be done on the timing chains.