

## Introduction

High speed digitizers find applications in several fields ranging from the industry to the study of nuclear and particle properties. In many cases complex measurement systems are implemented, which are composed by segmented or multiple detectors. These systems may require several acquisition channels and electronics to process the information. Digitizers implement multiple input channels (e.g. CAEN V1720 contains 8 channels, V1740 contains 64 of them), but it may happen that more boards are needed to acquire all the information.

The CAEN digitizers are designed also to have logic inputs and outputs which allow to create systems where boards operate as an all one board with synchronous signal sampling and same time reference. To obtain this, boards need to be “synchronized”, that is board internal clocks are set synchronously and the time reference is set the same. The synchronization, in general, allows the user to acquire from N boards with Y channel each, like if they were just one board with (N x Y) channels.

The aim of the present note is to show how to synchronize two or more homogeneous<sup>1</sup> CAEN digitizers in a multi-board acquisition system. We describe the steps needed to synchronize a simple system, composed by two V1720. We are going now to illustrate a hardware and software setup which can be easily generalized to more complex cases.

This document reports three example of hardware configuration and their relative features. The technical procedures including software implementation and hardware connection is described more extensively in the Application Note AN 2086 available at the website [www.caen.it](http://www.caen.it).

## What does “synchronize” different boards mean?

It is possible to obtain the synchronization of a multi-board system with four main system settings.

### I. Same clock propagated to all boards.

The digitizers input and output connectors allows the clock distribution in daisy chain. One digitizer board generates its internal clock and distributes it by the use of external output connectors. Such board represents the master board of the acquisition system. The remaining boards through their input connectors are linked to the master board clock signal and act as clock slaves.

Each board contains a Phase Lock Loop (PLL) which synthesizes the board clock either from an internal oscillator or from an external clock reference. Together with a programmable phase adjust it is possible to compensate for the delay in the propagation of the clock signal from a board to the other. In this way it is possible to align the clock of each board.

### II. Same time reference for all boards.

In normal applications, all boards belonging to an acquisition system have to start with the same time reference. For this reason input and output connectors are used to synchronize the start of the data taking and the time reference. The start logic signal can be propagated in daisy chain to all boards belonging to the acquisition system. The propagation of the start signal introduces a delay along the digitizer chain. This can be compensated introducing time offsets in the data acquisition start.

### III. Trigger propagation and/or correlation.

Digitizers are able to receive external trigger signals and propagate them outside. This allows e.g. to propagate a global trigger signal in daisy chain when events of interest have to be recorded.

Moreover the event selection can be either due to a input signal crossing the threshold set on its acquisition channel (channel auto-trigger) or to the output of logic<sup>2</sup> algorithms: e.g. the FPGA can be programmed to require that more than one channel registered signals over the threshold (majority operator). This feature allows to implement more complex trigger selections which can be used in case of more complex systems where the correlation between different subunits has to be considered.

### IV. Readout synchronization and event alignment<sup>3</sup>

For most of applications, all the digitizers of an acquisition system have to keep their memory buffers available for the storage of new information at the same time. The CAEN digitizers can implement a mechanism that prevents an asynchronous data taking, which may happen when at least one of the boards enters in a busy condition. The digitizer boards have BUSY IN/OUT and VETO IN/OUT connectors, which allow to stop the data acquisition and restore the system synchronization.

## Board Clock, Trigger Logic and Sampling

The sampling clock of the CAEN digitizer V1720 is either locked to an internal oscillator or to an external clock source. We will later see that this clock signal is generated and distributed to the different components of the digitizer.

<sup>1</sup>This application note does not show how to synchronize a number of non-homogeneous set of CAEN digitizers (V1724 + V1720 for instance). Even if non-homogeneous configuration can be in principle implemented, it has issues due to different clock speed that are not tackled in this document.

<sup>2</sup>The current firmware release allows to the require the majority logic operation.

<sup>3</sup>New firmware currently under test, the matter is not described in this document.

The event time tag, also called “trigger time tag” (TTT) is given by a counter which marks the arrival time of an external trigger signal or the time when a signal crosses the relative threshold set. For digitizers V1720 it is expressed in units of its clock cycles, 8 ns, corresponding to a frequency of 125 MHz. However, when the acquired data is written into the board internal memory, the TTT counter is read every 2 trigger logic clock cycles, which means that the trigger time stamp has an effective resolution of 16 ns.

The trigger logic algorithms operates at a frequency that is 125 MHz, while the ADC sampling frequency is 250 MHz. Boards other than the V1720 have different characteristic clock frequencies. Table 1 summarizes the clocks of digitizers V1720, V1751, V1724 and V1740.

Digitizer Model	Trigger Time Tag Resolution (ns)	Trigger Logic Cycle (ns)	Sampling Cycle (ns)
V1720	16	8	4
V1751	16	8	1
V1724	20	10	10
V1740 <sup>4</sup>	32	16	16

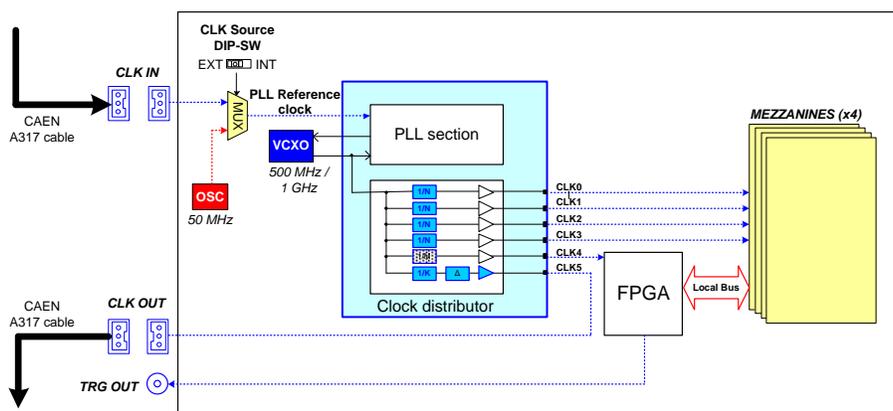
**Table 1. Characteristic clocks of CAEN digitizer V1720, V1751, V1724 and V1740.**

The present note is based on the synchronization of digitizers CAEN model V1720, with Firmware Release 3.4 or successive. The same firmware requirements apply to digitizers V1751/x24.

## Clock Synthesis and Distribution

Figure 1 reports a simplified sketch of the digitizers clock synthesis and distribution. We report here a brief description of the hardware components and their operations.

- In CAEN digitizers the clock management is provided by a PLL (Phase-locked Loop) and a Clock Distributor. The PLL can receive a reference clock from either an internal oscillator or an external clock source through the clock input (CLK-IN) connector. A mechanic switch on the board allows to select the clock generator.
- The role of the PLL is therefore to align the phase of a Voltage Controlled Crystal Oscillator (VCXO) to the reference one.
- The clock generated by the VCXO is passed to the Clock Distributor, which splits the clock signal in different branches. Each branch but one is sent to board subsystems: the main board FPGA and the mezzanines (which contain ADC’s, FPGA’s and memory buffers). The remaining branch is connected to the clock output (CLK OUT) connector. The Clock Distributor can send a different sub multiple of the VCXO frequency to each branch.
- The Clock Distributor can also apply a delay to the CLK OUT connector. This is a key feature of the synchronization since it can compensate the effect of the clock shift due to the clock daisy chain between different boards.



**Figure 1: Representation of the clock signal synthesis and distribution in the digitizer boards.**

<sup>4</sup> Clock conditions under PLL mode acquisition, see Technical Information Manual of the V1740.

## Clock Synchronization

The first action to be performed to obtain the synchronization of the acquisition system is the synchronization of the clock and its phase alignment. The hardware setup in represented in Figure 2.

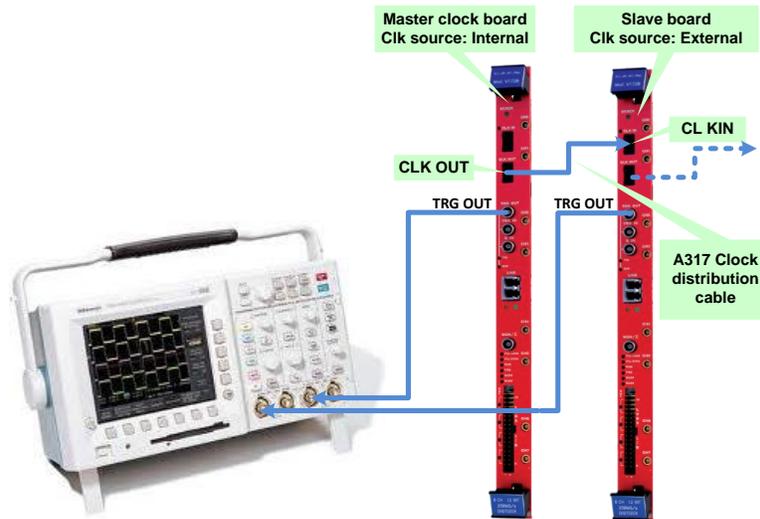


Figure 2: Sketch of the hardware setup needed for the synchronization of the board clock signals.

In the multi-board acquisition system, the master board (hereafter Master), will act as clock master providing a reference clock to the other one, that therefore will be a clock slave (hereafter Slave). With **CAENUpgrader** software (available at [www.caen.it](http://www.caen.it)) we can configure the Master PLL in order to enable the output of the clock (e.g. 62.5 MHz) and configure the Slave PLL in order to accept the external clock (setting identical frequencies). Then the Master CLK OUT should be connected to the Slave CLK IN using the cable A317. The TRG OUT connector of both boards can be programmed to deliver the clock signal. Connecting the TRG OUT of both boards to an oscilloscope with cables of equal length (50  $\Omega$  termination required) it is possible to observe the frequency of the clock signals. At first stage the clock signals should have the same frequency, but could appear out of phase as shown in Figure 3 on the left.

The CAEN digitizers allow to set a delay to the clock output that is useful to align the board clock signals in a multi-board acquisition system. In this hardware configuration the **CAENUpgrader** can program a delay in the Master clock output and align the Slave clock. If the delay is correctly set the signals should appear as on the right side of Figure 3.



Figure 3: Clock signals of the master and the slave board as they appear at the oscilloscope. On the left is represented the situation in which the two clocks have the same frequency, but are out of phase. On the right the clock signals are correctly synchronized.

## Example 1: External Trigger Propagation

This section will describe how to synchronize different boards **where the trigger comes from an external source and is propagated along the system through a daisy chain**. An external trigger source generates the trigger signal to be fed in the Master input.

The setup (shown in Figure 4) is such that:

- the external trigger goes to TRG IN of the Master;
- the daisy chain TRG IN/TRG OUT propagates the trigger and the start for the data acquisition;
- the signal source is the fan out of two of a function generator, synchronized with the trigger source, sent to one channel of each board with cables of equal length.

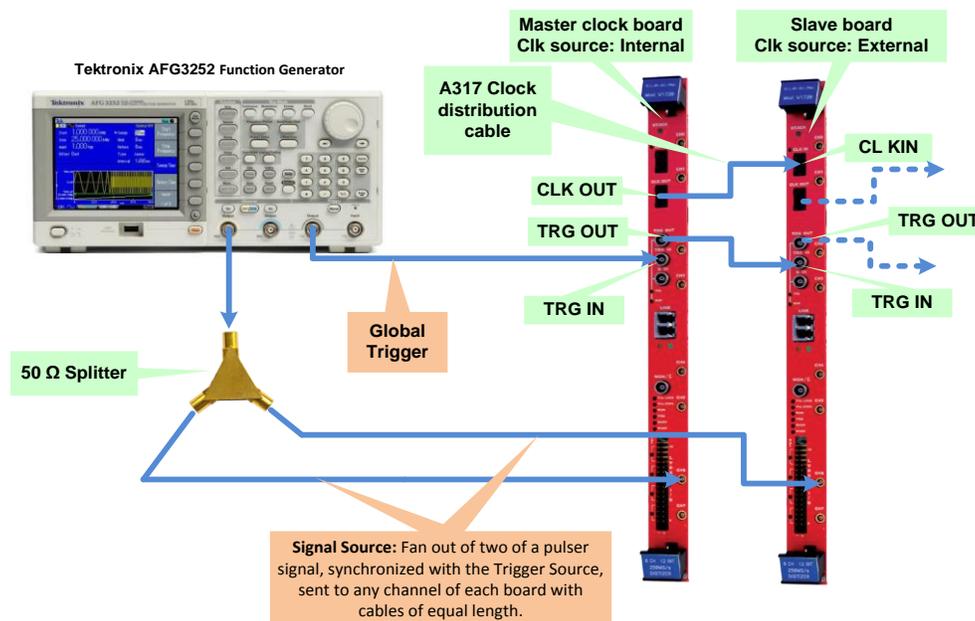


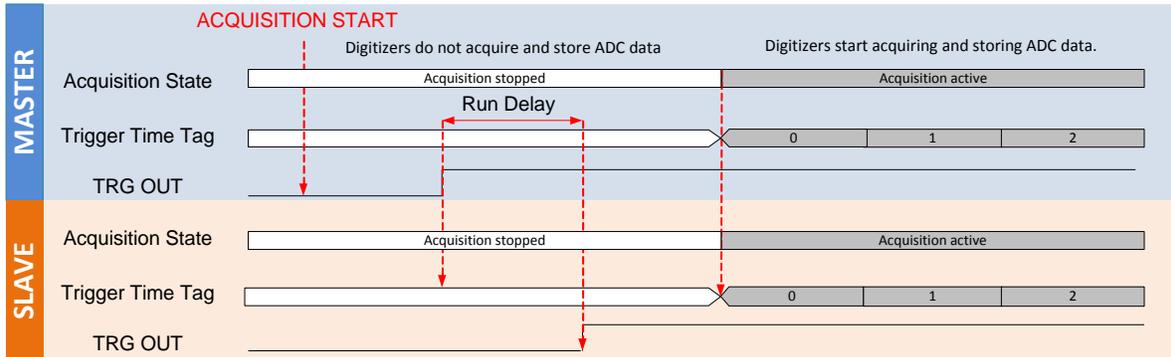
Figure 4: Hardware setup. Connection of boards and function generator.

The start of the event acquisition happens in the following way:

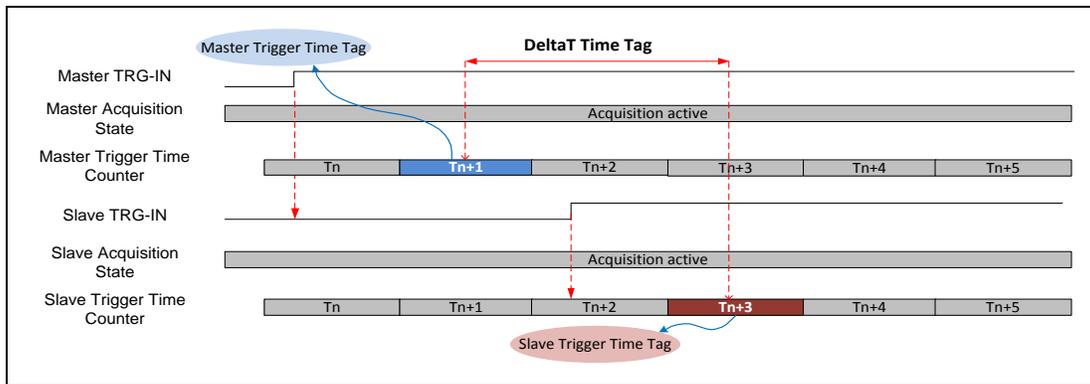
- all Slave boards armed to start with TRG IN edge, while the Master waits for a software (SW) trigger ;
- a SW trigger is sent to the Master and is propagated through the daisy chain TRG IN/TRG OUT and starts all the boards. In this way a delay may be present in the time reference of the boards (explanation in the next paragraphs);
- at this point Master is programmed in order to accept trigger on the TRG IN connector. The external trigger signals go through the daisy chain and trigger the event acquisition in all boards.

The daisy chain propagates the trigger signal from the Master to the Slave. The SW trigger that starts the acquisition arrives to the Slave with a delay proper of this hardware configuration. To ensure that all digitizers start the acquisition at the same time a delay in the start of the event acquisition can be set for the Master. This feature can be generalized to a hardware system with multiple boards. Figure 5 represents the timing of the SW trigger and the acquisition start of a system with 2 boards. It is possible to program the correct delay to obtain the time alignment of the board acquisition start: this will ensure that they will have the same time reference. Note in Figure 5, that the trigger time tag (TTT) of different digitizers start at the same time.

In this hardware setup the digitizers are configured such that the signals from the external global trigger (received after the SW trigger start) are considered for the event acquisition. The trigger signal sent to the Master is propagated to the Slave in daisy chain, so the latter will receive the trigger signal with a fixed delay compared to the Master. All boards start the acquisition synchronously and have the same time reference, so the trigger propagation introduces a delay also in the TTT of the events acquired by the Slave. Figure 6 represents the resulting TTT recorded by the boards.

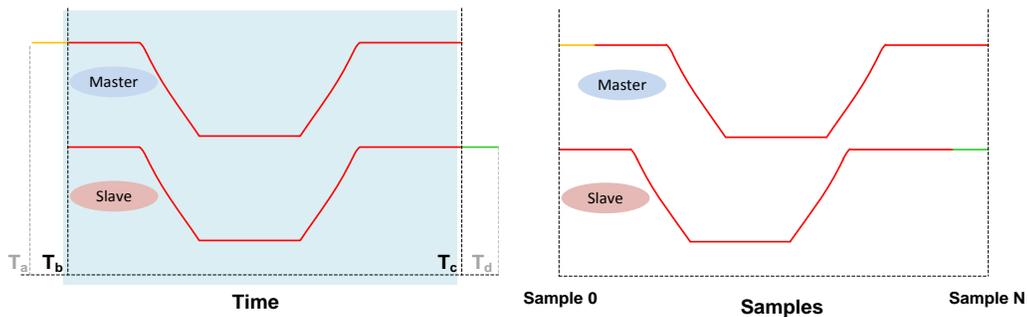


**Figure 5: Timing diagram of the start of run sequence**



**Figure 6: Synchronous Master and Slave acquisition (note that the Trigger Time Tags are different)**

The memory buffer of the digitizers record the events with a timing that is given by the arrival of the trigger signal. The delay in the TTT of the Slave implies that its memory buffer contains the sampling information that is out of phase compared to the one of the Master. Figure 7 better explains the delay introduced in the memory buffer of the Slave.



**Figure 7: SyncTest plot of the Master and Slave acquisition in the time frame on the left; in the buffer frame on the right.**

This misalignment is consequence of this hardware setup which propagates the trigger signal in daisy chain. The delay cannot generally be cured, and it is important to keep it low so that important waveform information is not lost.

## Example 2: Independent Channel Triggers

This section describes the synchronization of two boards **with independent channel triggers** (logic OR of the channel auto-triggers and independent external triggers). The aim is to align the start command and then let the boards trigger independently. Triggers won't be propagated, but the run start will be propagated through the daisy chain TRG OUT and the start input (S IN). **The Setup** shown in Figure 8 is such that:

- the daisy chain TRG OUT/S IN propagates the start of the acquisition;
- the signal source comes from the fan out of two of a function generator, sent to each board with cables of equal length.

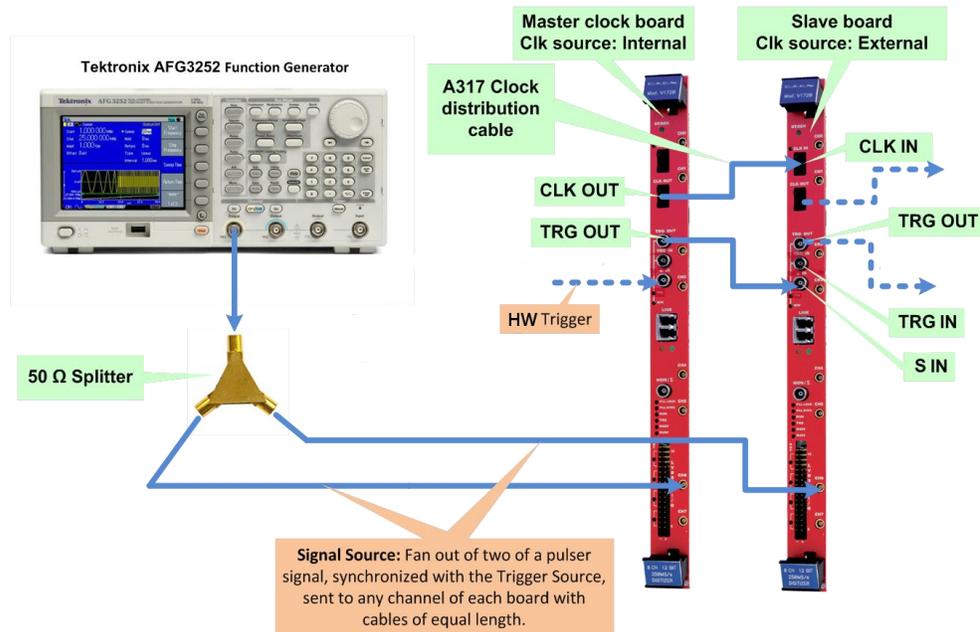


Figure 8: Example of hardware setup for synchronization.

The start of the event acquisition happens in the following way:

- the boards are programmed to start when a signal is fed in the S IN and to propagate the S IN input to the TRG OUT;
- the SW trigger is fed into the Master and is propagated through the daisy chain TRG OUT/S IN and start all the boards;
- each board triggers by the logic OR of the channel auto-triggers and the external TRG IN.

Optional: a HW trigger can be issued with a timer unit (e.g. CAEN V993) connected to the S-IN of the Master board. The Master board is turned in run mode with a logic high state and the data acquisition stops with the logic low state.

As in the previous example there is a delay in the acquisition start signal which propagates through the daisy chain from the Master to the Slave. The correct **start delay** should be set to synchronize the digitizer acquisition and the time stamp.

## Example 3: Trigger from External Logic Unit

This section shows how to synchronize the acquisition of two or more boards when one of their channels satisfies the trigger condition. This is obtained through the use of the logic OR of **all channels auto-triggers** given as trigger input to all boards. **The setup** shown in Figure 9 is such that:

- the TRG OUT of each board is connected with cables of equal length to the input of a logic unit (e.g. CAEN V976);
- the fan out of two of the logic unit output is connected to the TRG IN of each board with cables of equal length;
- signal source comes from the fan out of two of a function generator and is sent to each board with cables of equal length;
- optionally a timer unit (e.g. CAEN V993) can be connected to the logic unit input to generate the HW trigger.

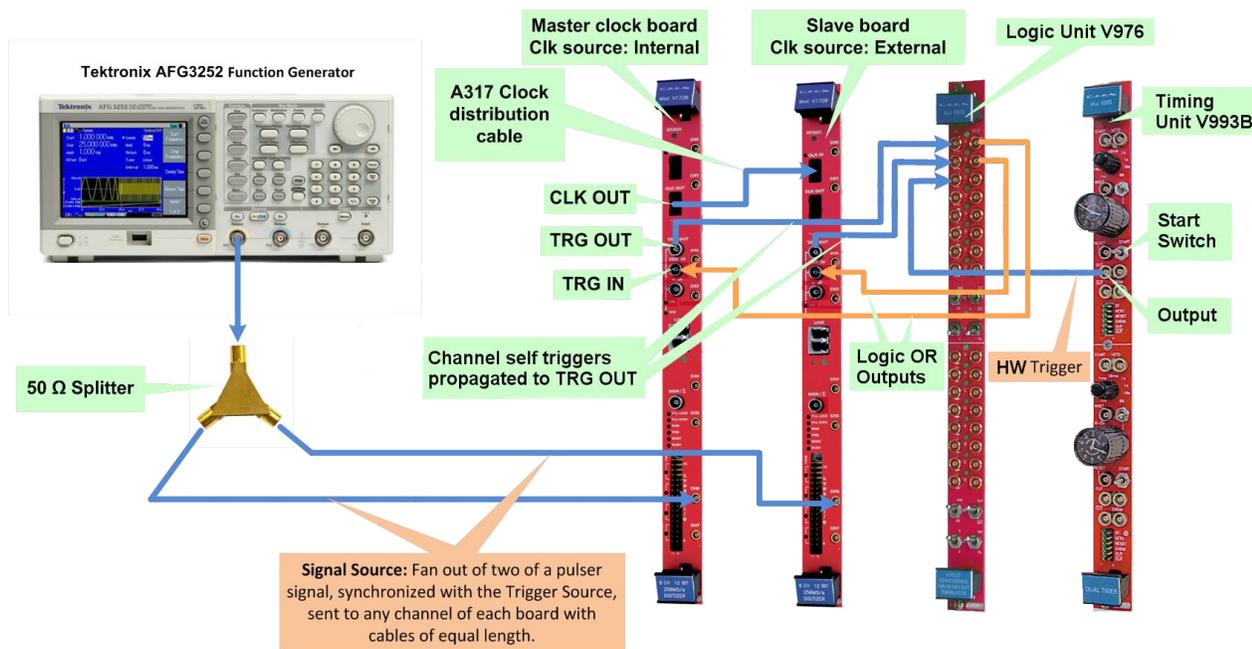


Figure 9: Hardware setup. Connection of boards and function generator.

The start of the event acquisition happens in the following way:

- all boards are armed to start the acquisition when a signal is fed into TRG IN;
- all boards are programmed to propagate the channel auto-trigger to the TRG OUT without triggering the event acquisition;
- all boards are programmed to trigger when an external trigger signal is received through the TRG IN;

In this hardware setup the trigger which starts the data acquisition is propagated to all the boards with the approximately the same time delay. With cables of equal length the board acquisition start is normally synchronous. However the start could be rarely asynchronous, in particular when the trigger signal is given in proximity of trigger clock edges.

A SW trigger can be also issued. In this configuration the Master board propagates the SW trigger to the TRG OUT and gives a logic signal high as input in the logic OR. All boards start the acquisition at the same time when the output of the logic unit is received.

In this example, differently from the previous ones, it is not necessary to set the **RUN delay** for the synchronization between digitizers. All digitizers start acquisition at the same time.